Gate resistor installed Dual N-channel MOS FET

For lithium-ion secondary battery protection circuits

General Features

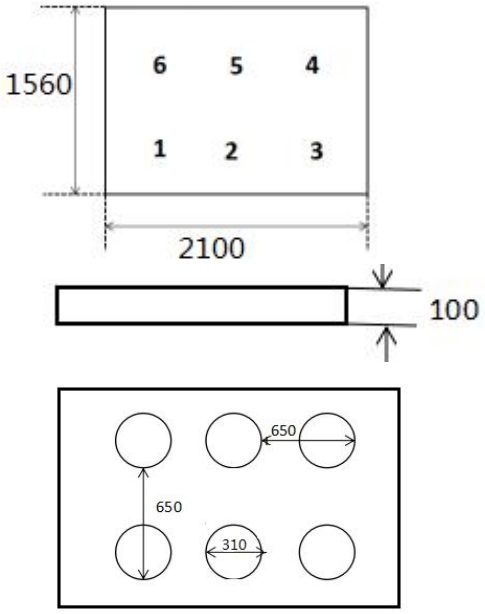
- Low source-source ON resistance:Rss(on) typ. = 10 mΩ, (VGS = 4.5 V)
- CSP(Chip Size Package)
- RoHS compliant (EU RoHS / MSL:Level 1 compliant)

Marking Symbol:16

Packaging

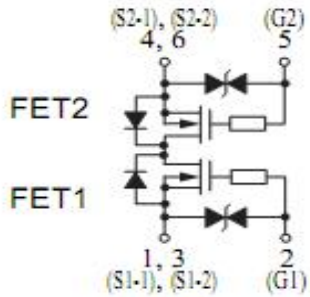
●Embossed type (Thermo-compression sealing) : 10000pcs / reel (standard)

Unit um



1.Source1-1(FET1)	4 Source2-1(FET2)
2.Gate1(FET1)	5.Gate2(FET2)
3.Source1-2(FET1)	6 Source2-2(FET2)

Equivalent circuit



Absolute Maximum Ratings Ta = 25℃

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		VDS	12	V
Gate-source Voltage *3		VGS	+/-10	V
Source Current	DC *1	IS1	6	A
	Pulse*2	ISp	60	A
Total Power Dissipation	DC *1		0.45	W
Channel Temperature		Tch	150	℃

Storage Temperature Range		Tstg	-55 to +150	℃
Thermal resistance(ch-a)	DC *1	Rth1	278	℃/W

Note *1 Mounted on FR4 board (25.4mm X25.4mmX t1.0mm, 36um Copper)

*2 t = 10us, Duty Cycle ≤1 %

Electrical Characteristics Ta = 25 °C ±3 °C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source Breakdown Voltage	VDSS	IS = 250uA, VGS = 0 V	12			V
Zero Gate Voltage Source Current	ISSS	VSS = 12 V, VGS = 0 V			1	uA
Gate-source Leakage Current	IGSS	VGS = ±10 V, VSS = 0 V			±10	uA
Gate-source Threshold Voltage	Vth	IS = 250uA, VSS = 10 V	0.4	0.8	1.2	V
Source-source On-state Resistance	RSS(on)1	IS = 3.0 A, VGS = 4.5 V		10	13	mΩ
	RSS(on)2	IS = 3.0 A, VGS = 3.8 V		**11**	**15**	
	RSS(on)3	IS = 3.0 A, VGS = 2.5 V		15	19	
Body Diode Forward Voltage	VF(s-s)	IF = 1.0 A, VGS = 0 V		0.9	1.5	V
Input Capacitance *1	Ciss	VSS = 10 V, VGS = 0 V, f = 1 KHz		2335		pF
Output Capacitance *1	Coss			321		
Reverse Transfer Capacitance *1	Crss			244		
Turn-on delay Time *1,*2	td(on)	VGS = 4.5 V, VSS=10V, RL=3.3 Ω , IS=3A,RG=6Ω		680		ns
Rise Time *1,*2	tr			2960		
Turn-off delay Time *1,*2	td(off)	VGS = 4.5 V, VSS=10V, RL=3.3 Ω , IS=3A,RG=6Ω		6480		ns
Fall Time *1,*2	tf			6760		
Total Gate Charge *1	Qg	VG1S1 = 4.5 V, VSS = 10V, IS =6A		36		nC
Gate-source Charge *1	Qgs			5.6		
Gate-drain Charge *1	Qgd			8.0		

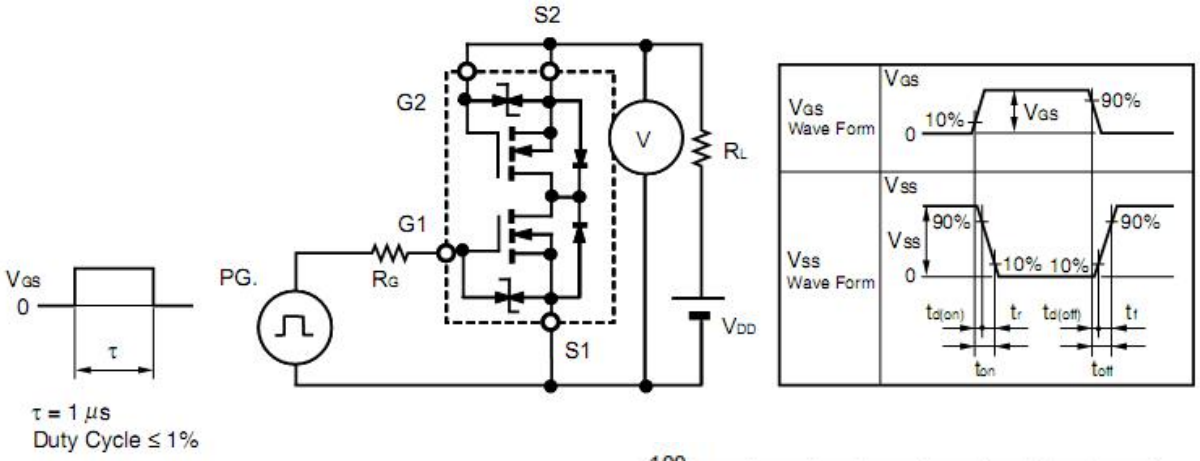
Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

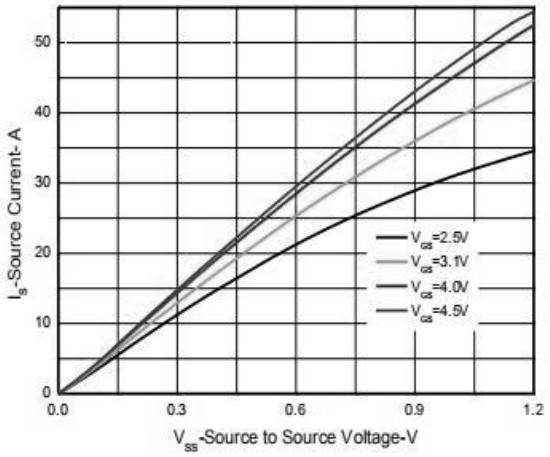
*1 Guaranteed by design, not subject to production testing

*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time

Note2:Measurement circuit

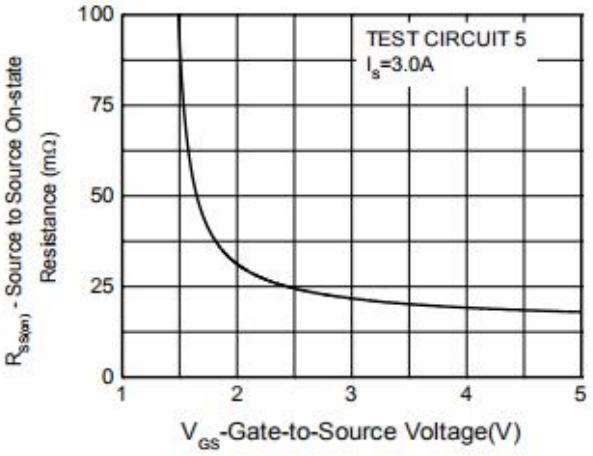
Technical Data (reference)





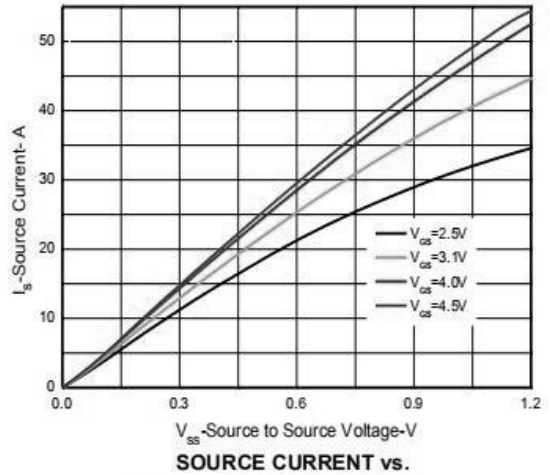
SOURCE CURRENT vs.

SOURCE TO SOURCE VOLTAGE



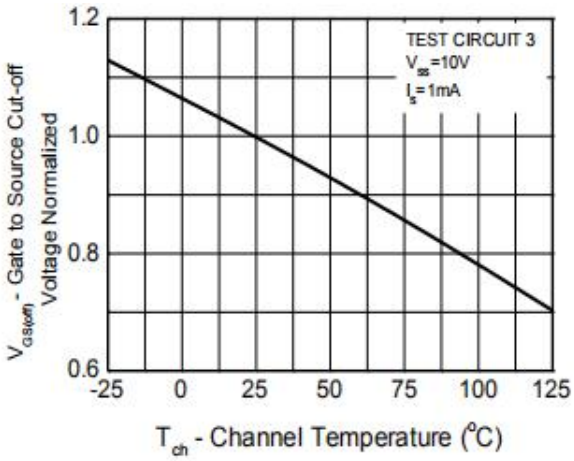
SOURCE TO SOURCE ON-STATE RESISTANCE vs.

GATE TO SOURCE VOLTAGE



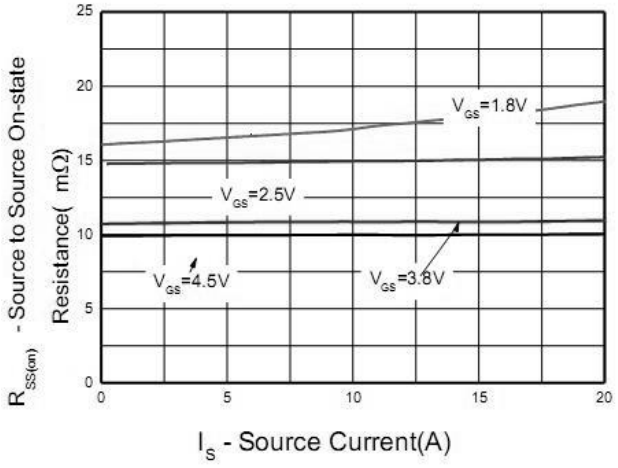
SOURCE CURRENT vs.

SOURCE TO SOURCE VOLTAGE

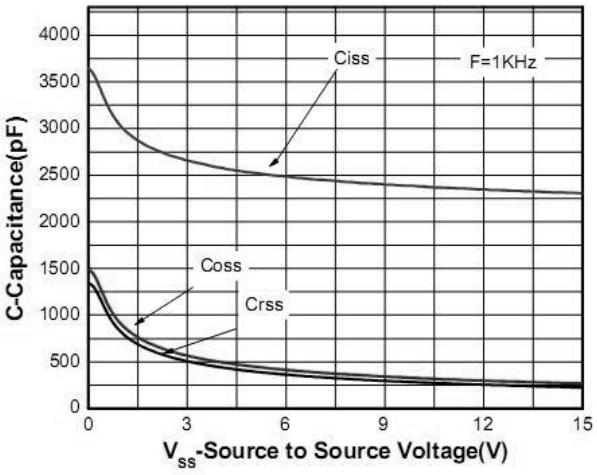


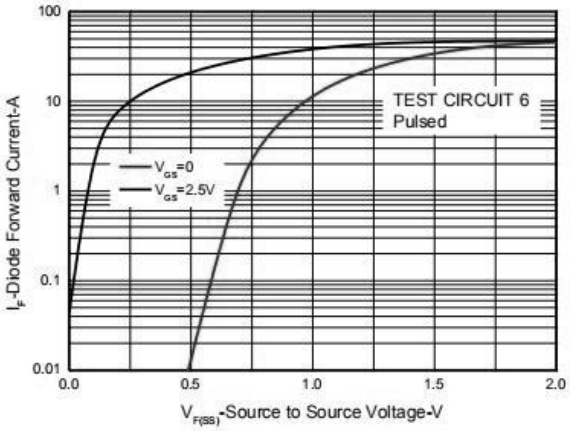
GATE TO SOURCE CUT-OFF VOLTAGE vs.

CHANNEL TEMPERATURE

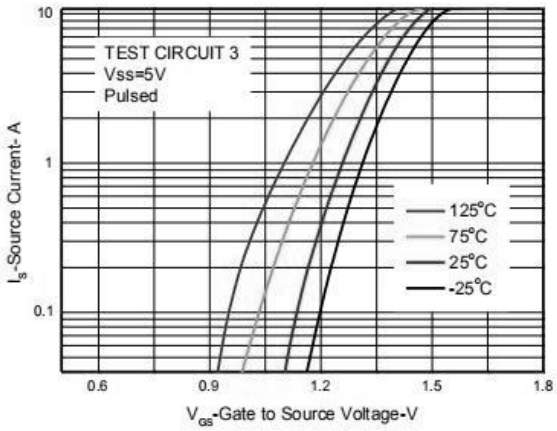


On-Resistance vs.Source current

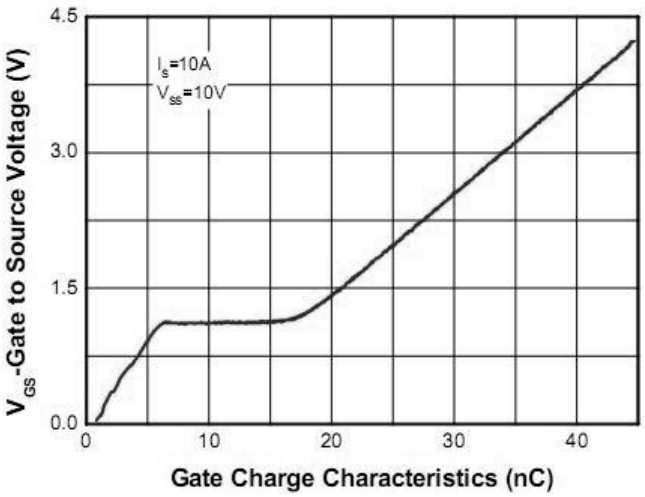




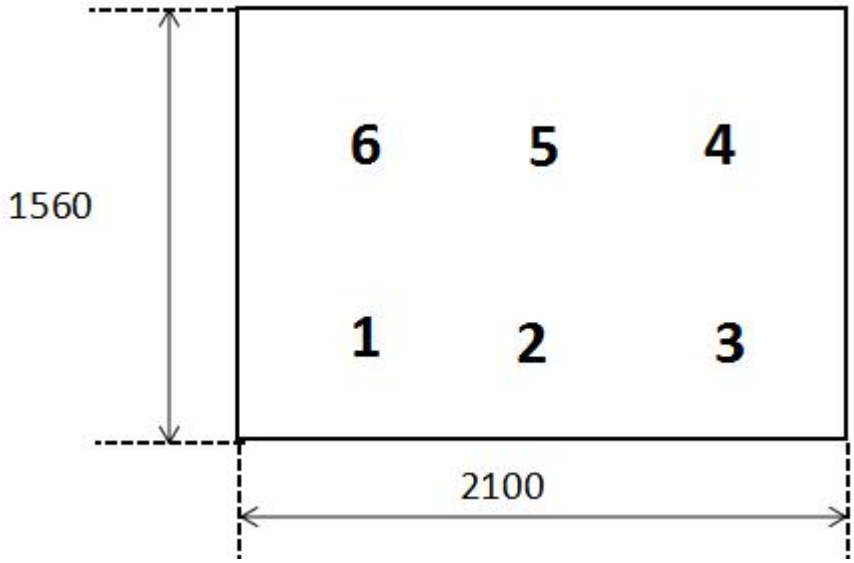
SOURCE TO SOURCE DIODE FORWARD VOLTAGE

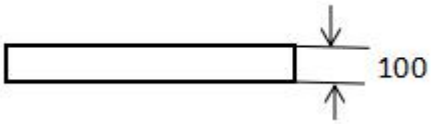


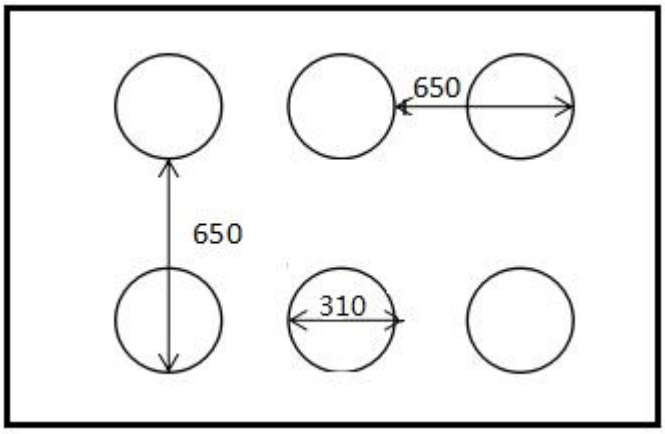
FORWARD TRANSFER CHARACTERISTICS



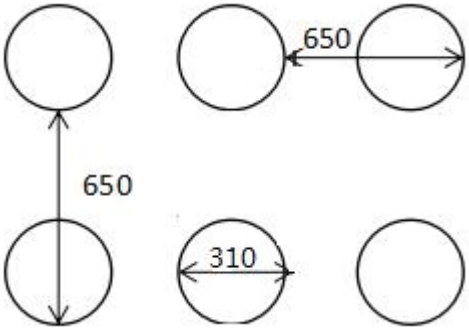
Chip Size Package **Unit: um**







Land Pattern (Reference) (Unit: um)



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