

### Gate resistor installed Dual N-channel MOS FET

For lithium-ion secondary battery protection circuits

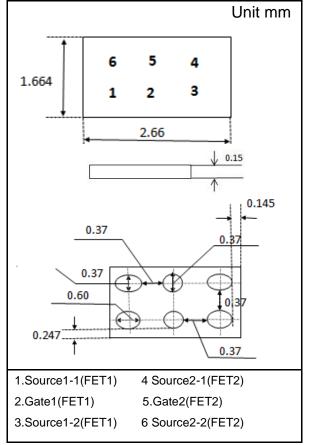
#### **General Features**

- Low source-source ON resistance:Rss(on) typ. = 3.8 mΩ,
  (VGS = 4.5 V)
- CSP(Chip Size Package)
- RoHS compliant (EU RoHS / MSL:Level 1 compliant)

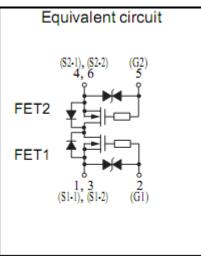
### Marking Symbol:16

#### Packaging

• Embossed type (Thermo-compressionsealing) : 5000pcs / reel (standard)



#### Absolute Maximum Ratings Ta = 25℃ Parameter Symbol Rating Unit Drain-Source Voltage VDS 12 V VGS V Gate-source Voltage \*3 +/-12 DC \*1 IS1 15 А Source Current Pulse\*2 80 ISp A W **Total Power Dissipation** DC \*1 PD1 0.45 **Channel Temperature** Tch 150 °C -55 to Storage Temperature Range °C Tstg +150 Thermal resistance(ch-a) DC \*1 °C/W Rth1 278



Note \*1 Mounted on FR4 board (25.4mm X25.4mmX t1.0mm, 36um Copper)

\*2 t = 10us, Duty Cycle  $\leq$ 1 %



#### Electrical Characteristics Ta = 25 °C ±3 °C

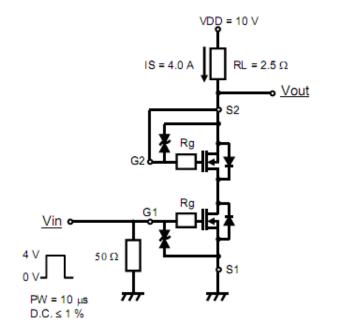
Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Drain-source Breakdown Voltage	VDSS	IS = 1 mA, VGS = 0 V	12			V
Zero Gate Voltage Source Current	ISSS	VSS = 12 V, VGS = 0 V			1.0	uA
Gate-source Leakage Current	IGSS	$VGS = \pm 10 V$ , $VSS = 0 V$			±100	nA
Gate-source Threshold Voltage	Vth	IS = 0.5 mA, VSS = 10 V	<b>0.</b> 4	0.7	10	V
Source-source On-state Resistance	RSS(on)1	IS = 4.0 A, VGS = 4.5 V		3.8	5.0	mΩ
	RSS(on)2	IS = 4.0 A, VGS = 2.5 V		6.0	9.0	
Body Diode Forward Voltage	VF(s-s)	IF = 4.0 A, VGS = 0 V		0.8	1.2	V
Input Capacitance	Ciss	VSS = 10 V, VGS = 0 V, f = 1 MHz		2760		pF
Output Capacitance	Coss			450		
Reverse Transfer Capacitance	Crss			390		
Turn-on delay Time	td(on)	VDD = 10 V, VGS = 0 to 4.0 V		4.1		μs
Rise Time	tr	IS = 4.0 A		5.2		
Turn-off delay Time	td(off)	VDD = 10 V, VGS = 4.0 to 0 V		12.9		μs
Fall Time	tf	IS = 4.0 A		8.3		
Total Gate Charge	Qg	VDD = 10 V		26		nC
Gate-source Charge	Qgs	VGS = 0 to 4.0 V,		9		
Gate-drain Charge	Qgd	IS = 4.0 A		8		

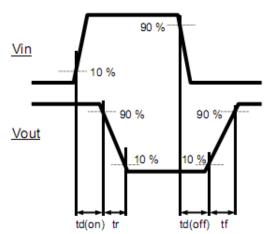
Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

\*1 Guaranteed by design, not subject to production testing

\*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time

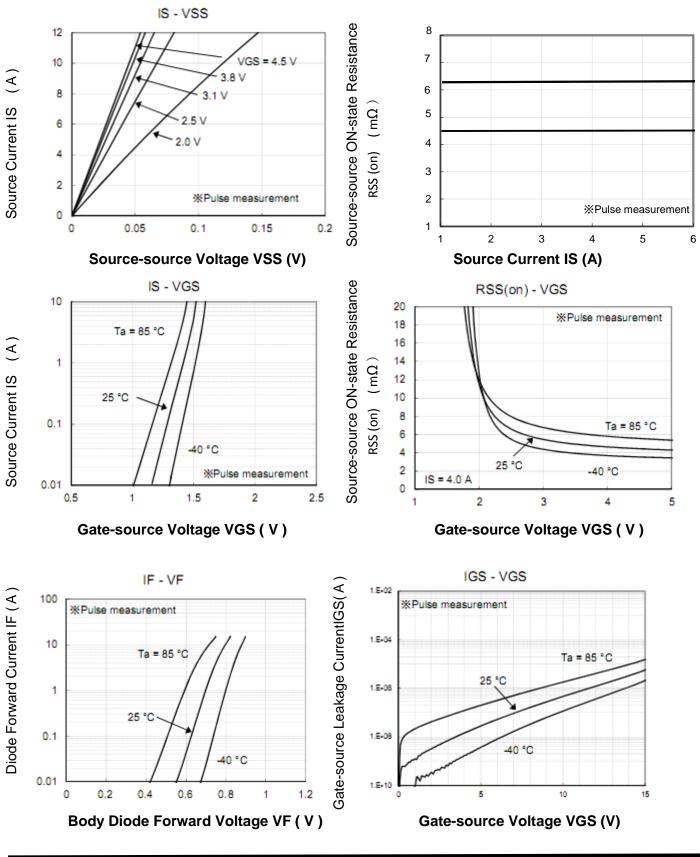
Note2:Measurement circuit



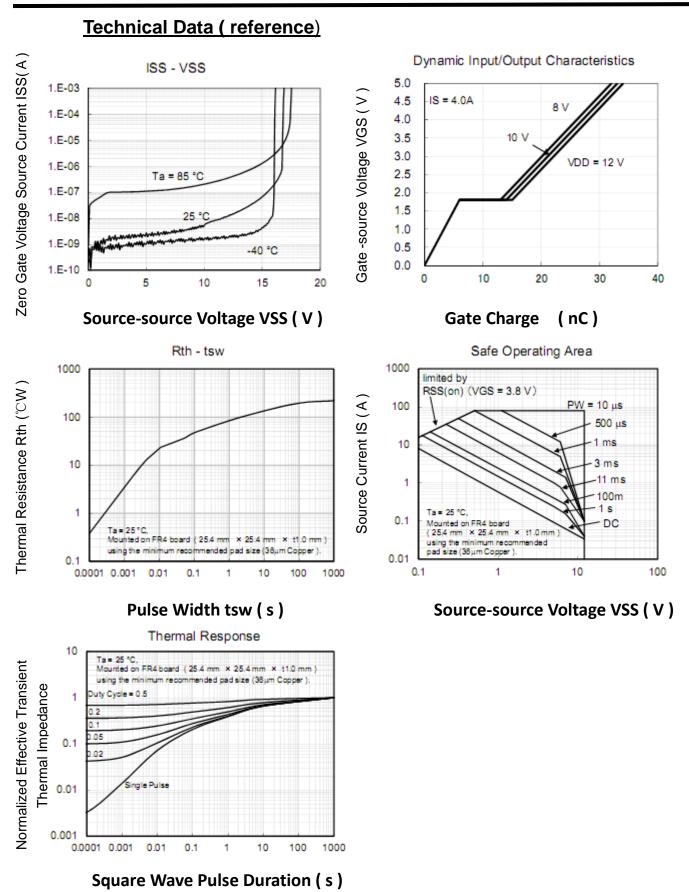








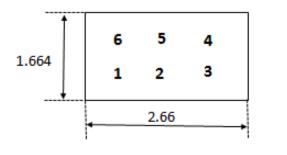




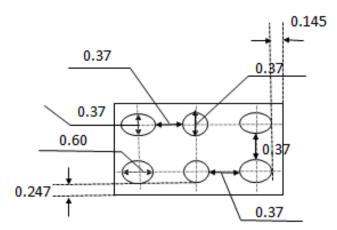


# **Chip Size Package**

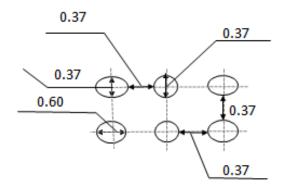
# Unit: mm







# Land Pattern (Reference) (Unit: mm)





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