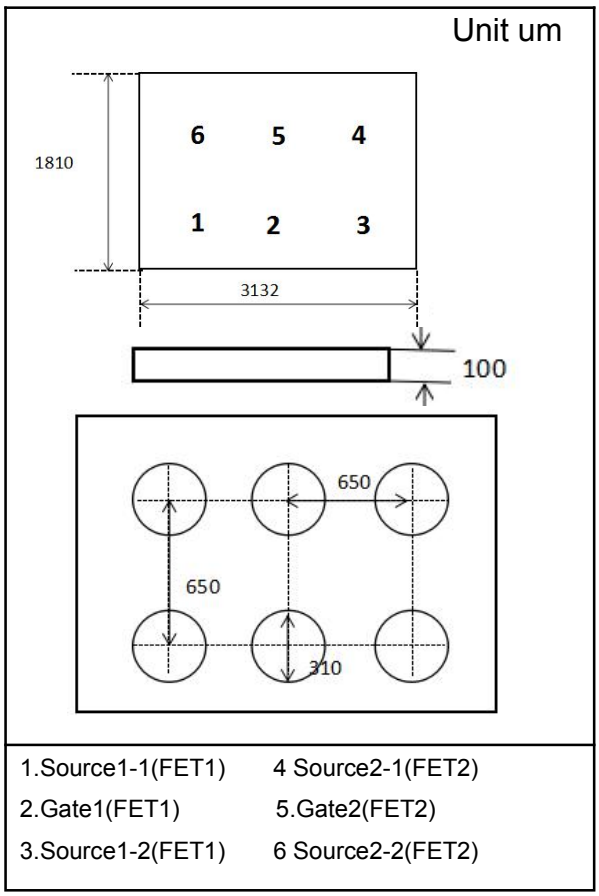
Gate resistor installed Dual N-channel MOS FET

For lithium-ion secondary battery protection circuits



1.Source1-1(FET1)	4 Source2-1(FET2)
2.Gate1(FET1)	5.Gate2(FET2)
3.Source1-2(FET1)	6 Source2-2(FET2)

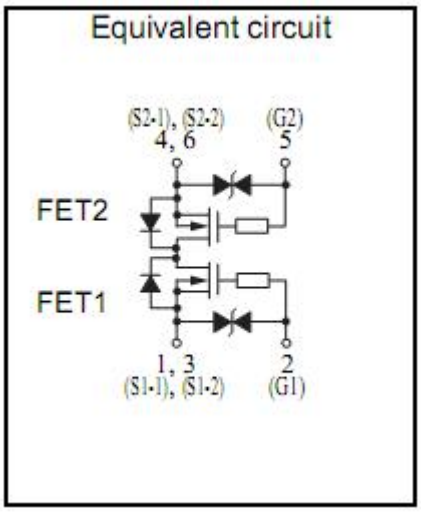
General Features

- Low source-source ON resistance:Rss(on) typ. = 4.5 mΩ, (VGS = 4.5 V)
- CSP(Chip Size Package)
- RoHS compliant (EU RoHS / MSL:Level 1 compliant)

Marking Symbol:16

Packaging

●Embossed type (Thermo-compression sealing) : 10000pcs / reel (standard)



Absolute Maximum Ratings Ta = 25℃

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		VDS	12	V
Gate-source Voltage *3		VGS	+/-10	V
Source Current	DC *1	IS1	8	A
	Pulse*2	ISp	80	A
Total Power Dissipation	DC *1	PD1	0.45	W

Channel Temperature		Tch	150	℃
Storage Temperature Range		Tstg	-55 to +150	℃
Thermal resistance(ch-a)	DC *1	Rth1	278	℃/W

Note *1 Mounted on FR4 board (25.4mm X25.4mmX t1.0mm, 36um Copper)

*2 t = 10us, Duty Cycle ≤1 %

Electrical Characteristics Ta = 25 °C ±3 °C

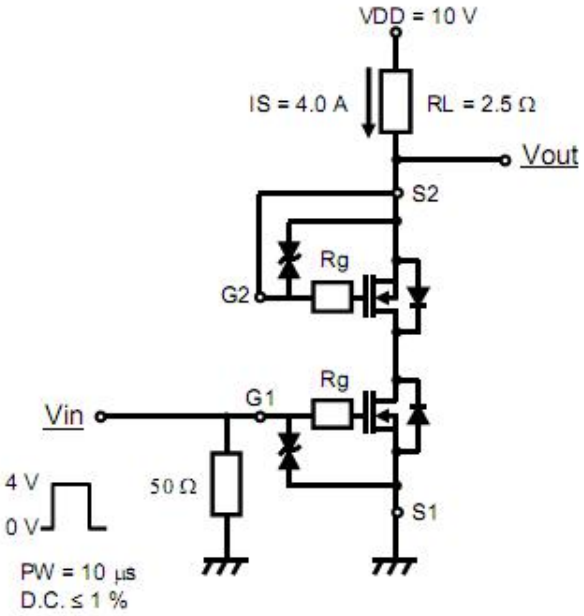
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source Breakdown Voltage	VDSS	IS = **250uA**, VGS = 0 V	12			V
Zero Gate Voltage Source Current	ISSS	VSS = 12 V, VGS = 0 V			1.0	uA
Gate-source Leakage Current	IGSS	VGS = ±10 V, VSS = 0 V			±10	uA
Gate-source Threshold Voltage	Vth	IS = **250uA**, VSS = 10 V	0.45	0.7	1.0	V
Source-source On-state Resistance	RSS(on)1	IS = 4.0 A, VGS = 4.5 V		4.5	5.7	mΩ
	RSS(on)2	IS = 4.0 A, VGS = 3.8 V		4.9	6.3	
	RSS(on)3	IS = 4.0 A, VGS = 2.5 V		6.5	11	
Body Diode Forward Voltage	VF(s-s)	IF = 8.0 A, VGS = 0 V		0.8	1.2	V
Input Capacitance *1	Ciss	VSS = 10 V, VGS = 0 V, f = 1 MHz		4360		pF
Output Capacitance *1	Coss			720		
Reverse Transfer Capacitance *1	Crss			670		
Turn-on delay Time *1,*2	td(on)	VDD = 10 V, VGS = 0 to 4.0 V		2.2		μs
Rise Time *1,*2	tr	IS = 4.0 A		5.3		
Turn-off delay Time *1,*2	td(off)	VDD = 10 V, VGS = 4.0 to 0 V		13.9		μs
Fall Time *1,*2	tf	IS = 4.0 A		12.1		
Total Gate Charge *1	Qg	VDD = 10 V		42		nC
Gate-source Charge *1	Qgs	VGS = 0 to 4.0 V,		14		
Gate-drain Charge *1	Qgd	IS = 4.0 A		13		

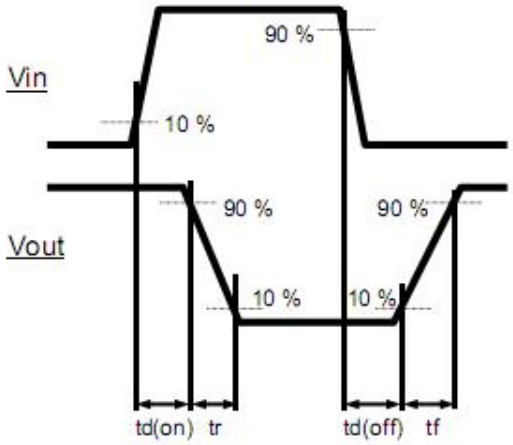
Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

*1 Guaranteed by design, not subject to production testing

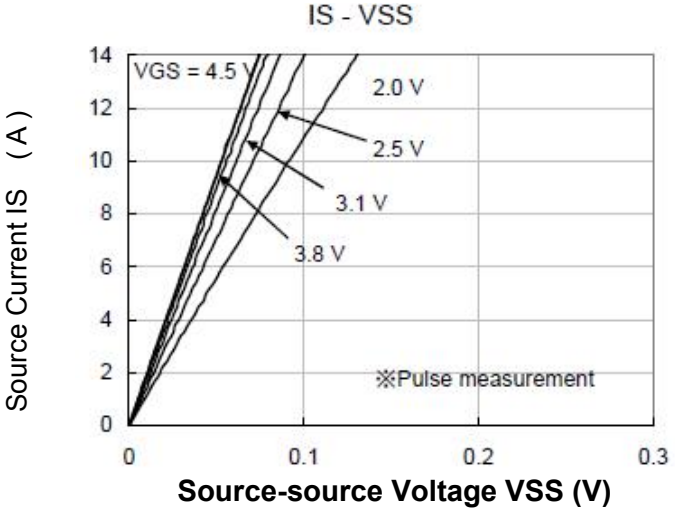
*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time

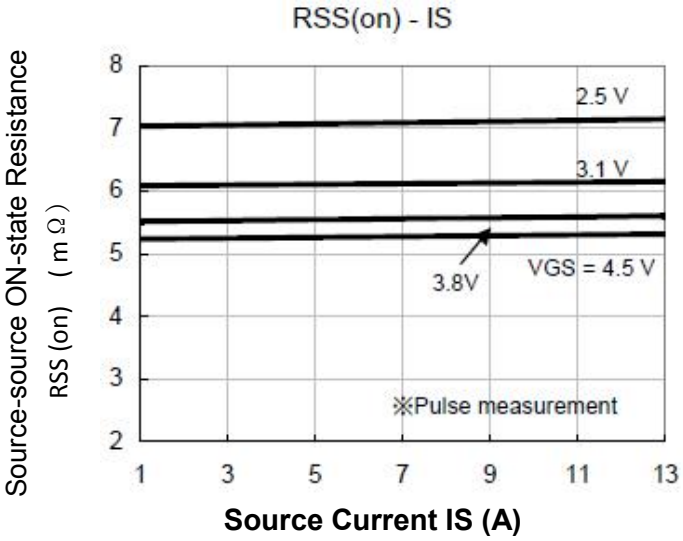
Note2:Measurement circuit

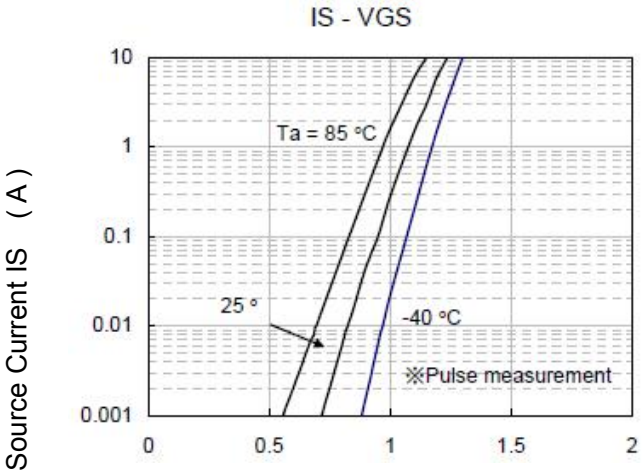


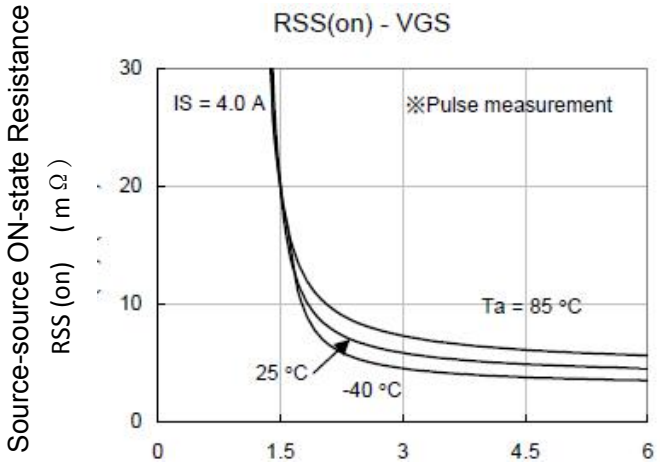


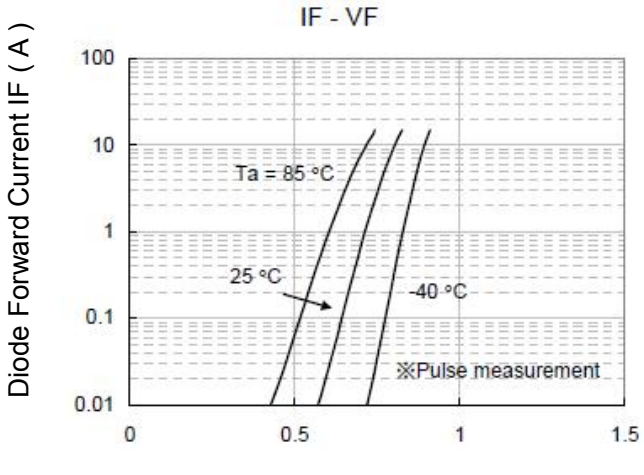
Technical Data (reference)

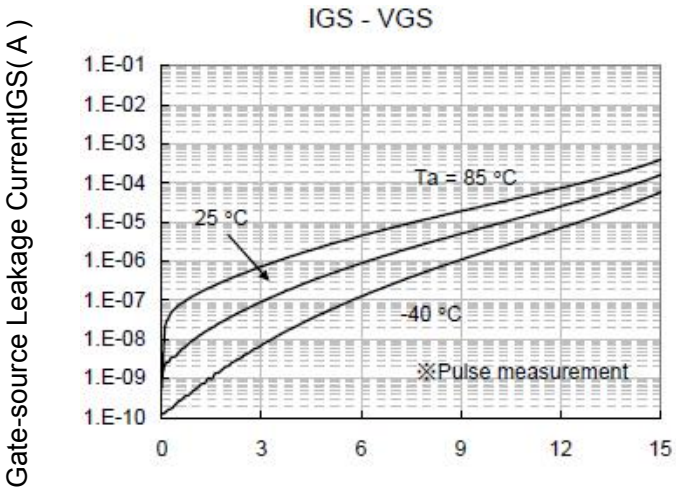




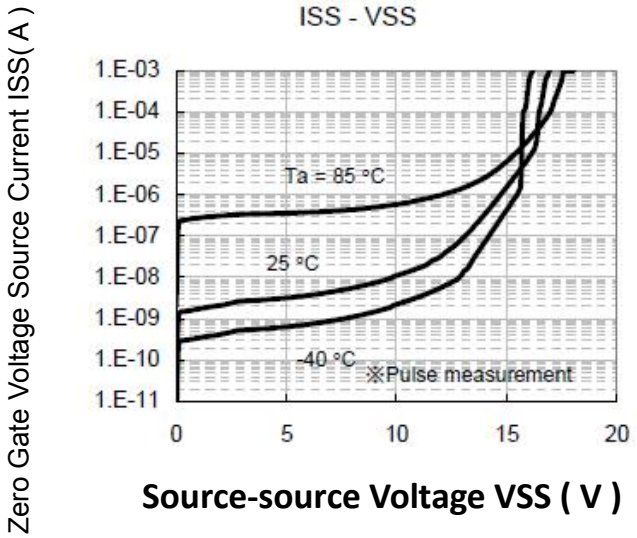


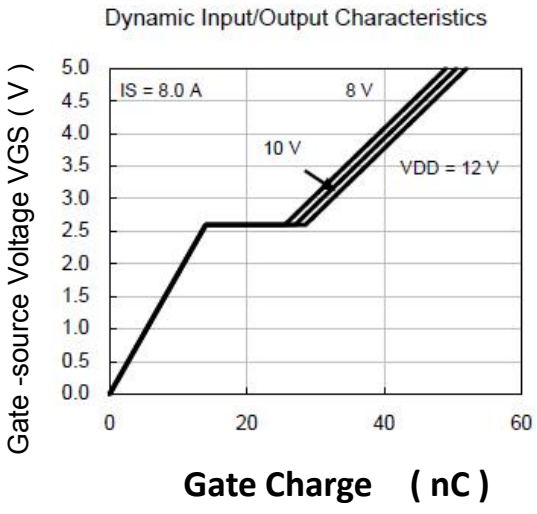


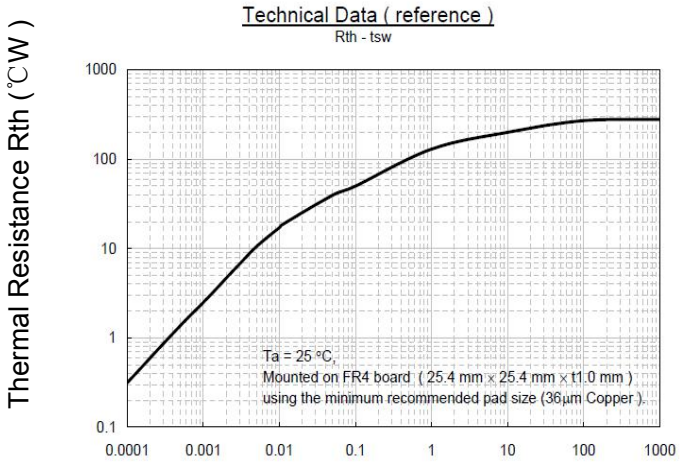


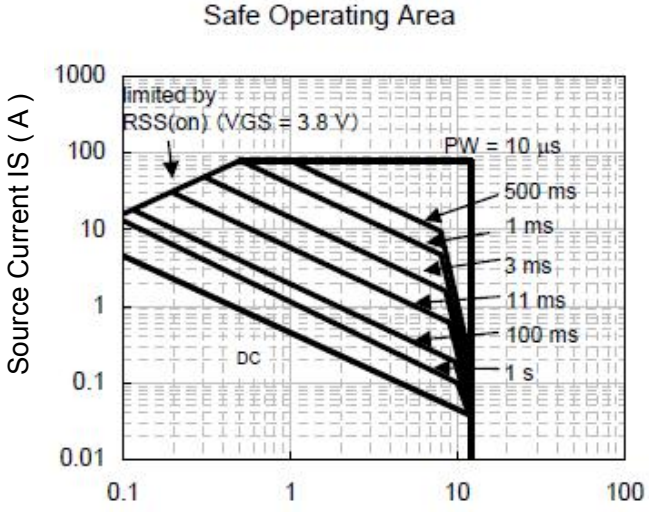


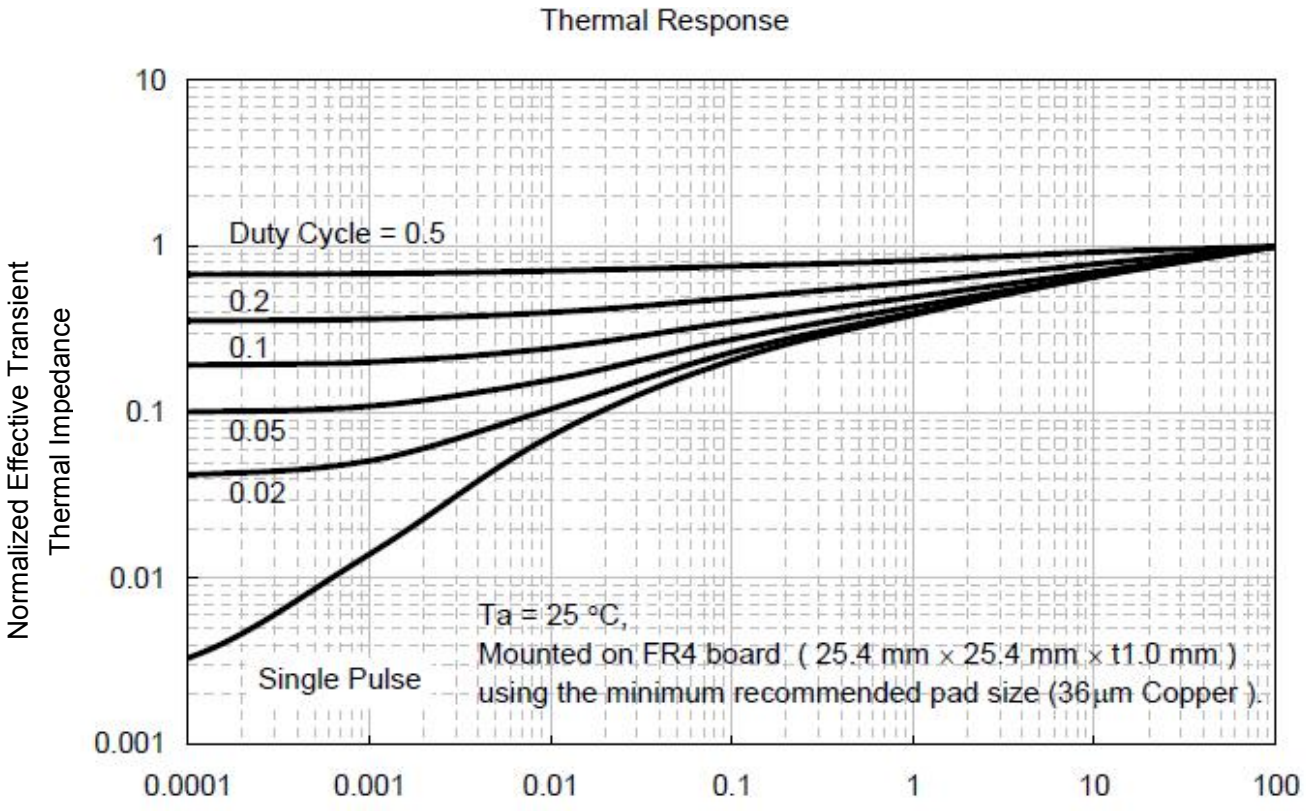
Technical Data (reference)



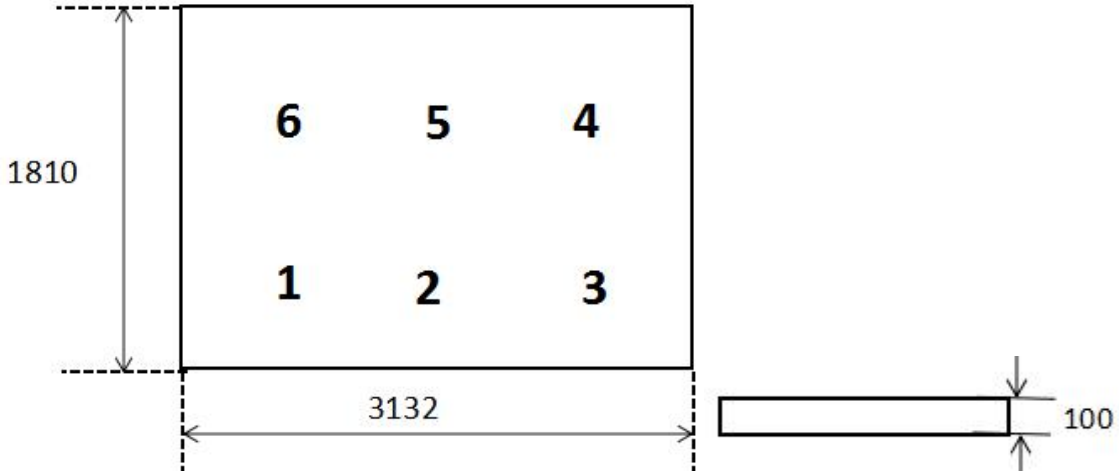


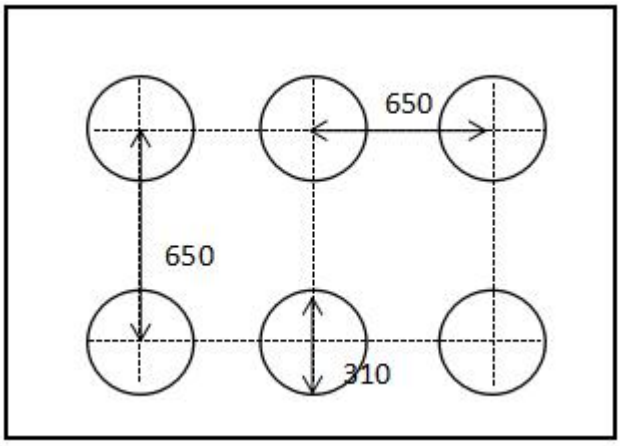

Technical Data (reference)
Rth - tsw
Thermal Resistance Rth (℃W)
1000
100
10
1
0.1
0.0001
0.001
0.01
0.1
1
10
100
1000
Ta = 25 °C,
Mounted on FR4 board (25.4 mm × 25.4 mm × t1.0 mm)
using the minimum recommended pad size (36μm Copper).
Pulse Width tsw (s)


Safe Operating Area
Source Current IS (A)
1000
100
10
1
0.1
0.01
0.1
1
10
100
limited by
RSS(on) (VGS = 3.8 V)
PW = 10 μs
500 ms
1 ms
3 ms
11 ms
100 ms
1 s
DC
Source-source Voltage VSS (V)

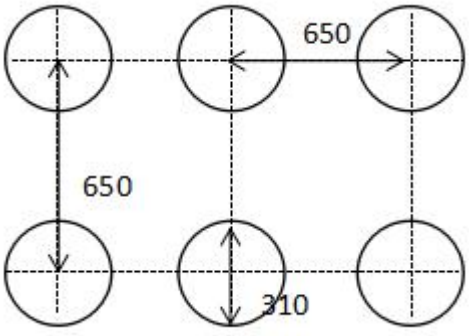

Thermal Response
Normalized Effective Transient
Thermal Impedance
10
1
0.1
0.01
0.001
0.0001
0.001
0.01
0.1
1
10
100
Duty Cycle = 0.5
0.2
0.1
0.05
0.02
Single Pulse
Ta = 25 °C,
Mounted on FR4 board (25.4 mm × 25.4 mm × t1.0 mm)
using the minimum recommended pad size (36μm Copper).
Square Wave Pulse Duration (s)

Chip Size Package **Unit: um**





and Pattern (Reference) (Unit: um)



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