

## FNK N-Channel Enhancement Mode Power MOSFET

### Description

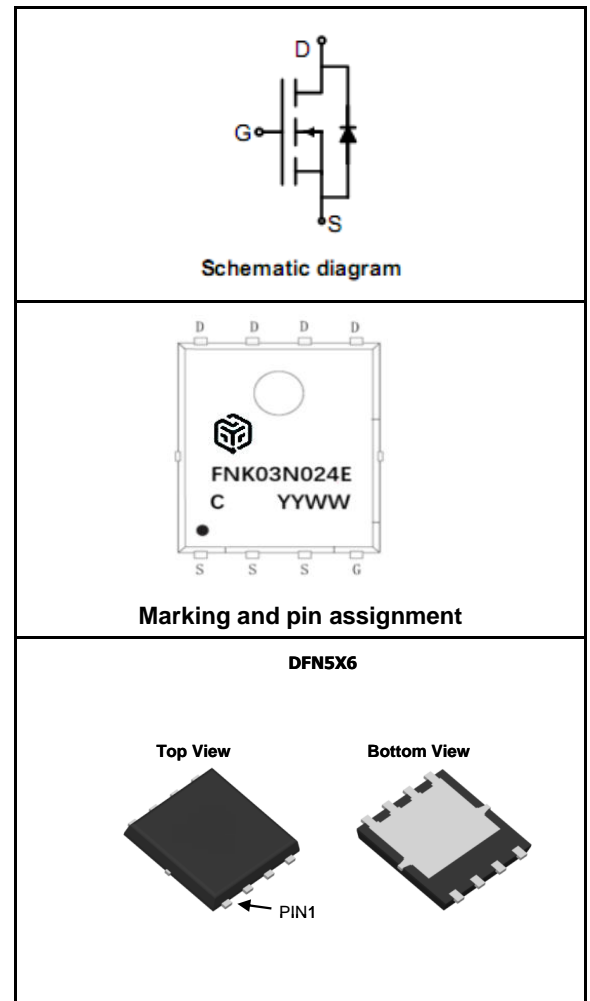
The FNK03N024E uses advanced trench technology and provide excellent  $R_{DS(ON)}$  with low gate charge, it can be used in a wide variety of applications.

### General Features

- $V_{DS} = 30V, I_D = 180A$   
 $R_{DS(ON)} < 2.4m\Omega @ V_{GS}=10V$   
 $R_{DS(ON)} < 5.0m\Omega @ V_{GS}=4.5V$
- High density cell design for ultra low  $R_{DS(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high EAS
- Excellent package for good heat dissipation

### Application

- Power switching application
- Hard switched and High frequency circuits
- Uninterruptible power supply



### PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
FNK03N024E	FNK03N024E	DFN5*6			

### ABSOLUTE MAXIMUM RATINGS( $T_A=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous@ Current-Pulsed (Note 1)	$I_D(25^{\circ}C)$	180	A
	$I_{DM}$	720	A
Maximum Power Dissipation	$P_D$	108	W
Single pulse avalanche energy(Note 5)	EAS	300	mJ

Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^{\circ}\text{C}$
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## THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	1.15	$^{\circ}\text{C/W}$
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## ELECTRICAL CHARACTERISTICS ( $T_A=25^{\circ}\text{C}$ unless otherwise noted)

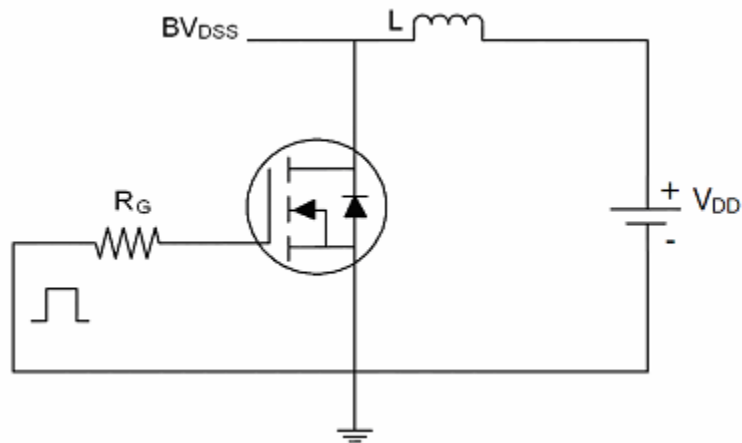
Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =250μA	30			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V			1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V			±100	nA
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0	1.5	2.5	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =10A		2.0	2.4	mΩ
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =6A		3.6	5.0	mΩ
DYNAMIC CHARACTERISTICS (Note4)						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, F=1.0MHz		4945		PF
Output Capacitance	C <sub>OSS</sub>			908		PF
Reverse Transfer Capacitance	C <sub>rss</sub>			493		PF
SWITCHING CHARACTERISTICS (Note 4)						
Delay Time	t <sub>d(on)</sub>	V <sub>DS</sub> =15V, V <sub>DS</sub> =10V, R <sub>GEN</sub> =6Ω R <sub>L</sub> =1Ω, ID=50A		19		nS
Turn-on Rise Time	t <sub>r</sub>			94		nS
Turn-Off Delay Time	t <sub>d(off)</sub>			28		nS
Turn-Off Fall Time	t <sub>f</sub>			30		nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =15V, I <sub>D</sub> =20A, V <sub>GS</sub> =10V		35		nC
Gate-Source Charge	Q <sub>gs</sub>			11		nC
Gate-Drain Charge	Q <sub>gd</sub>			10		nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =40A			1.2	V
Diode Forward Current (Note 2)	I <sub>S</sub>				40	A
Reverse Recovery Time	trr	T <sub>J</sub> = 25℃, I <sub>F</sub> =90A di/dt = 100A/us (Note3)		47		ns
Reverse Recovery Charge	Qrr			130		nc

## NOTES:

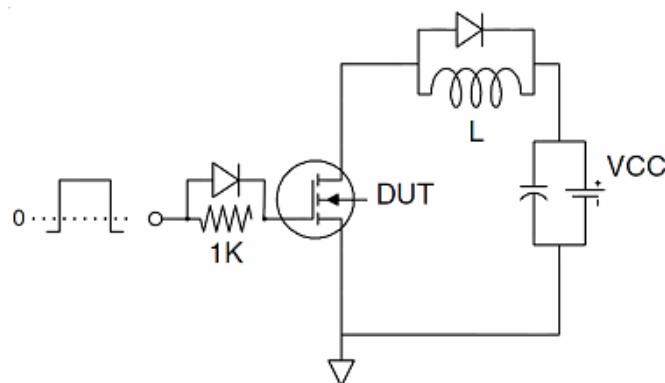
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on 1in<sup>2</sup> FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production testing
5. EAS condition  $T_J=25^{\circ}\text{C}$ ,  $V_{DD}=15V$ ,  $V_G=10V$ ,  $L=0.5mH$ ,  $R_g=25$

## Test circuit

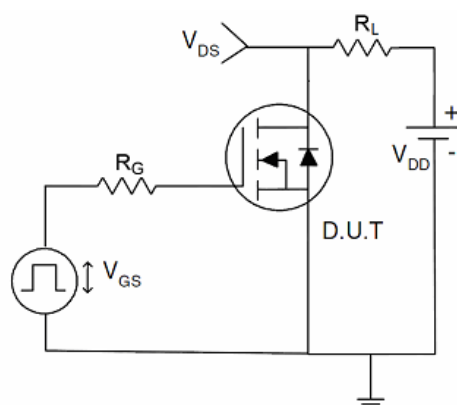
### 1) EAS test Circuits

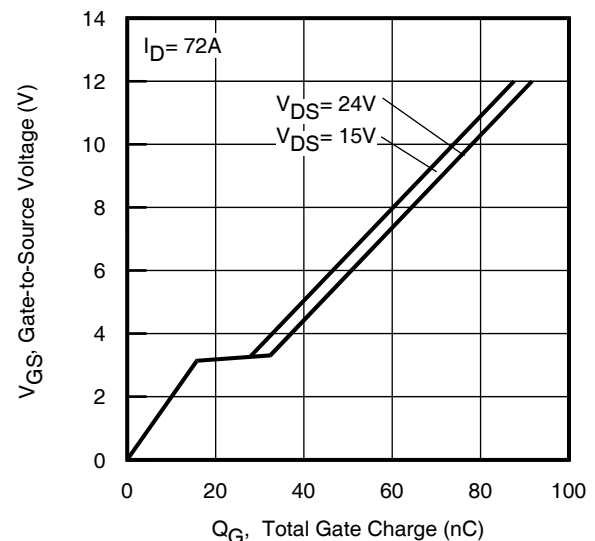
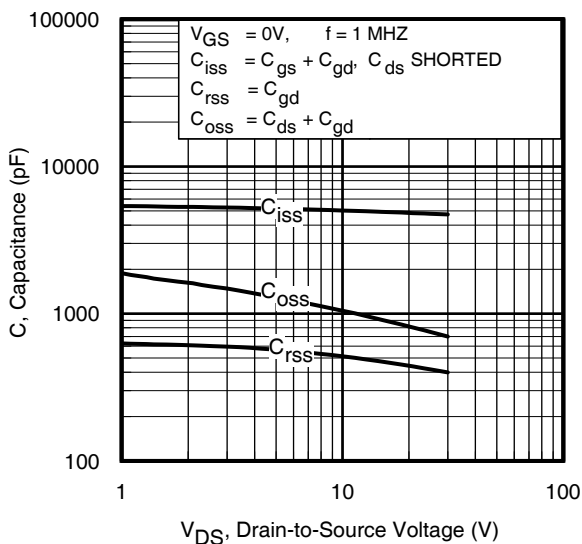
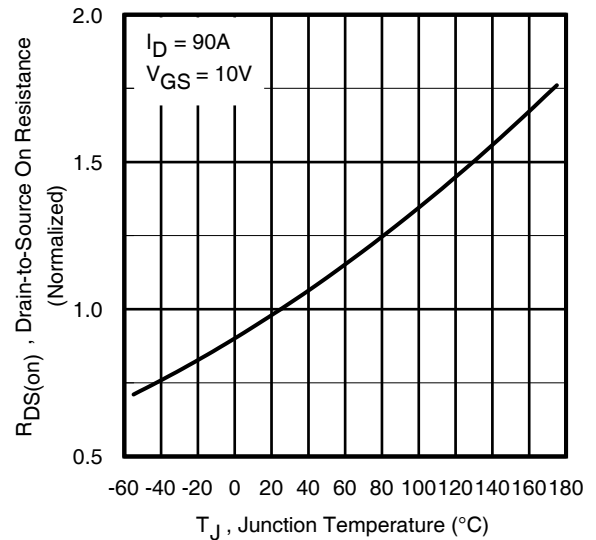
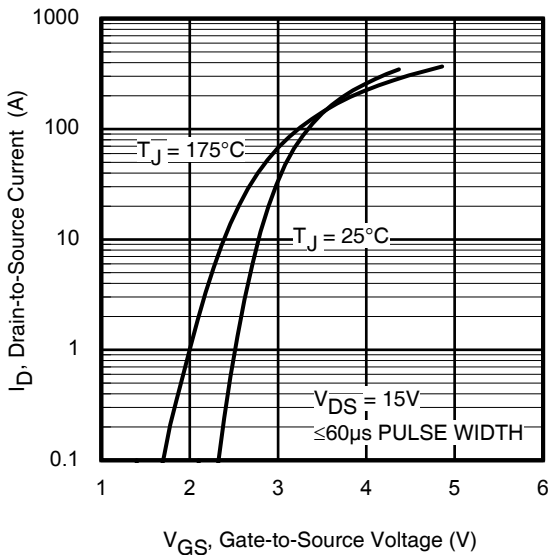
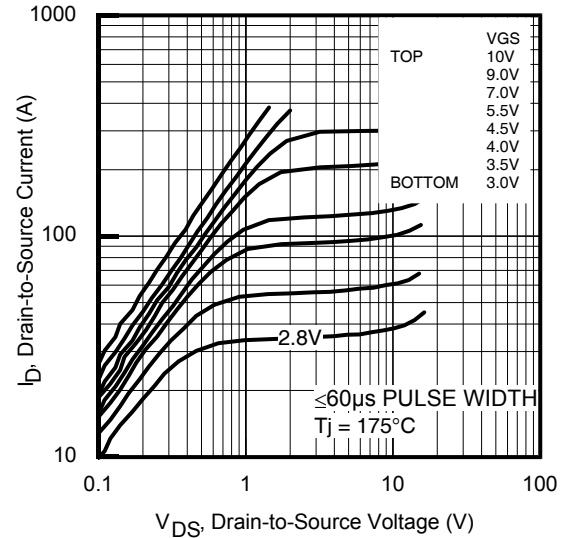
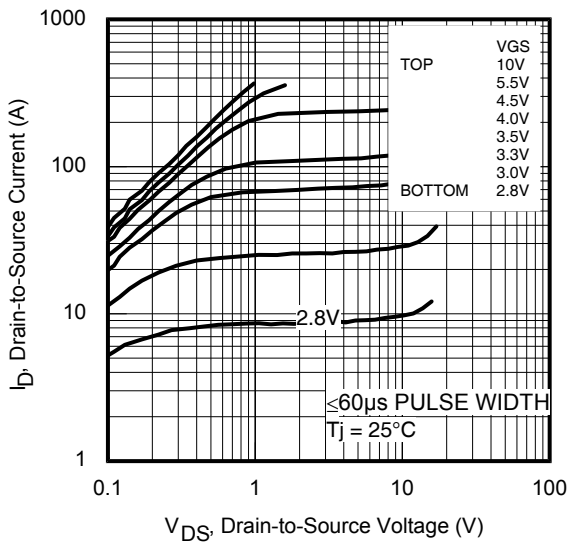


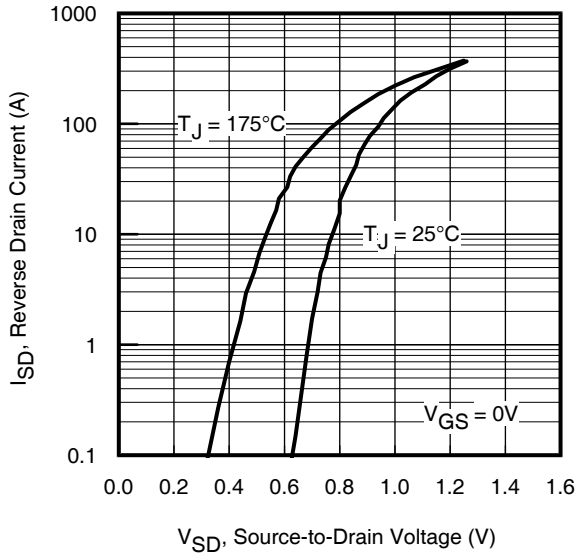
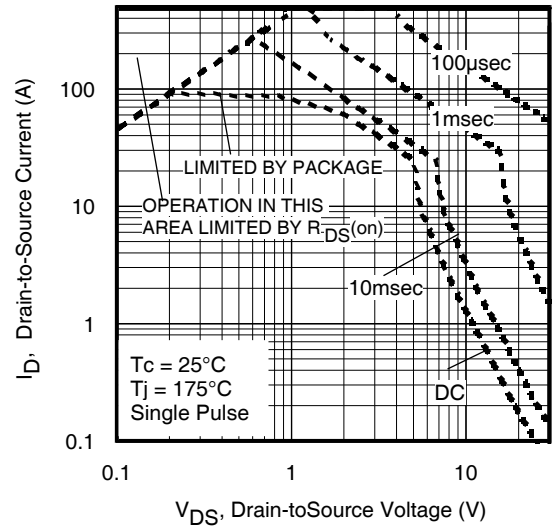
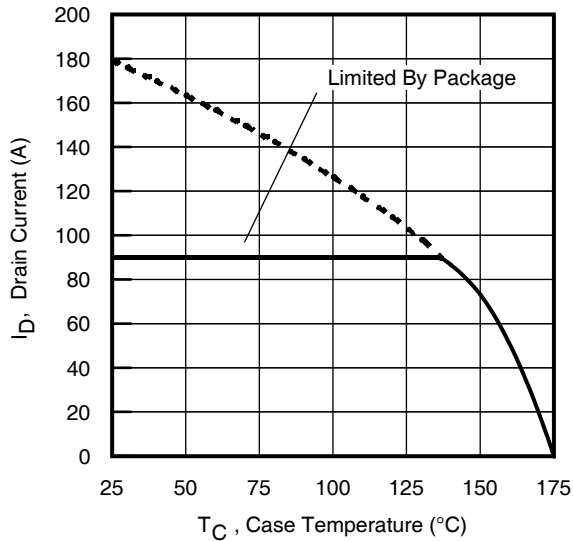
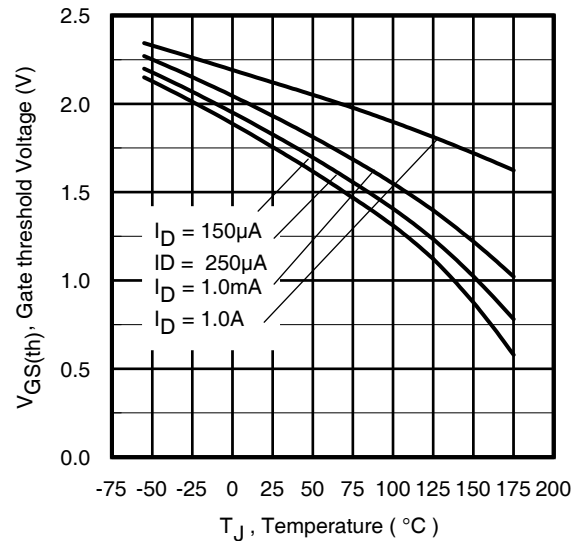
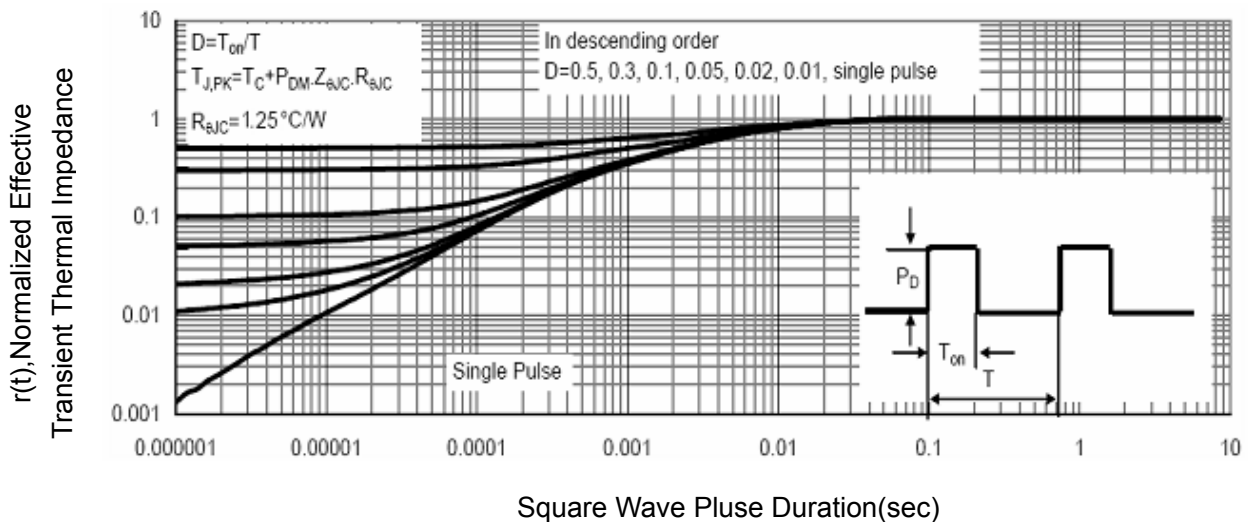
### 2) Gate charge test Circuit

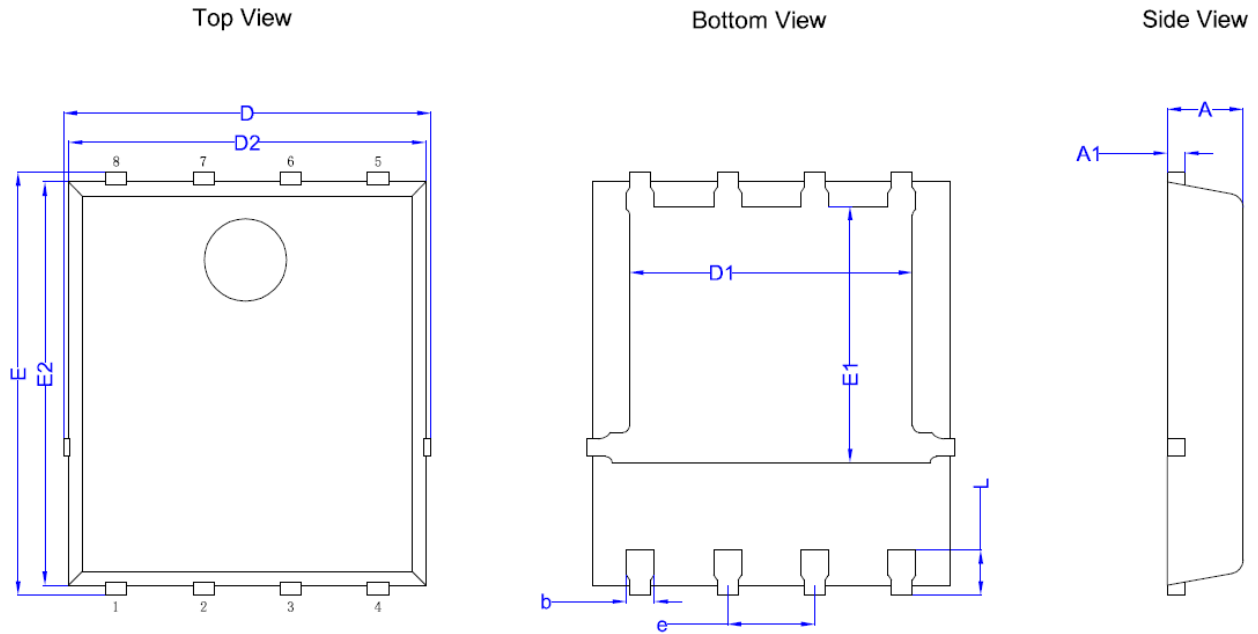


### 3) Switch Time Test Circuit



**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

**Fig 5. Typical Capacitance vs. Drain-to-Source Voltage**
**Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage**


**Fig 7. Typical Source-Drain Diode Forward Voltage**

**Fig 8. Maximum Safe Operating Area**

**Fig 9. Maximum Drain Current vs. Case Temperature**

**Fig 10. Threshold Voltage vs. Temperature**

**Figure 11 Normalized Maximum Transient Thermal Impedance**

**DFN5X6-8L Package Information**


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.00	1.10	1.20
A1	0.254 BSC		
D	5.15	5.35	5.55
E	5.95	6.15	6.35
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
e	1.27BSC		
b	0.31	0.41	0.51
L	0.56	0.66	0.76

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