

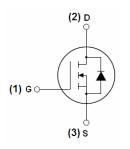
FNK N-Channel Enhancement Mode Power MOSFET

Description

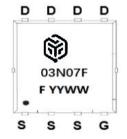
The FNK03N07F uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

- $V_{DS} = 30V, I_D = 75A$ $R_{DS(ON)} < 7.0 \text{m } \Omega \text{ @ } V_{GS} = 10V$ $R_{DS(ON)} < 11 \text{m} \Omega \text{ @ } V_{GS} = 4.5V$
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation
- Low RDSON



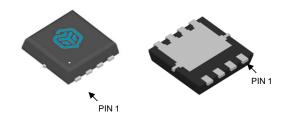
Schematic diagram



Marking and pin assignment

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



Top View

Bottom View

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
03N07F	FNK03N07F	DFN3.3*3.3	-	-	-

Absolute Maximum Ratings (T_A=25 ℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	30	V
Gate-Source Voltage	V _G S	±20	V
Drain Current-Continuous	I _D	75	А
Drain Current-Continuous(T _C =100 °C)	I _D (100℃)	50	А
Pulsed Drain Current	I _{DM}	300	А
Maximum Power Dissipation	P _D	83	W
Derating factor		0.56	W/℃
Operating Junction and Storage Temperature Range	T_{J}, T_{STG}	-55 To 175	°C



FNK03N07F

Thermal Characteristic

Electrical Characteristics (T_A=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Тур	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250µA	30	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V,V _{GS} =0V	-	-	1	μΑ
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	$V_{DS}=V_{GS}$, $I_{D}=250\mu A$	1.0	1.4	2.2	V
	R _{DS(ON)}	V _{GS} =10V, I _D =15A	-	5.8	7.0	mΩ
Drain-Source On-State Resistance		V _{GS} =4.5V, I _D =10A	-	9.8	11	
		V_{GS} =3.3V, I_{D} =5A		19.0	26	
Forward Transconductance	g FS	V _{DS} =5V,I _D =24A	20	-	-	S
Dynamic Characteristics (Note4)				I		
Input Capacitance	C _{lss}		-	830	-	PF
Output Capacitance	C _{oss}	V _{DS} =15V,V _{GS} =0V, F=1.0MHz	-	220	-	PF
Reverse Transfer Capacitance	C _{rss}	F=1.UMHZ	-	180	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}		-	6	-	nS
Turn-on Rise Time	t _r	V_{DD} =10 V , I_{D} =30 A	-	4	-	nS
Turn-Off Delay Time	t _{d(off)}	V_{GS} =10 V , R_{GEN} =2.7 Ω	-	18	-	nS
Turn-Off Fall Time	t _f		-	5	-	nS
Total Gate Charge	Qg	\/ -40\/ -20 4	-	45	-	nC
Gate-Source Charge	Q _{gs}	$V_{DS}=10V,I_{D}=30A,$ $V_{GS}=10V$	-	12	-	nC
Gate-Drain Charge	Q _{gd}	VGS-10V	-	8	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V,I _S =24A	-	-	1.2	V
Diode Forward Current (Note 2)	Is		-	-	80	Α
Reverse Recovery Time	t _{rr}	TJ = 25°C, IF = 80A	-	22	50	nS
Reverse Recovery Charge	Qrr	$di/dt = 100A/\mu s^{(Note3)}$	-	12	20	nC

Notes:

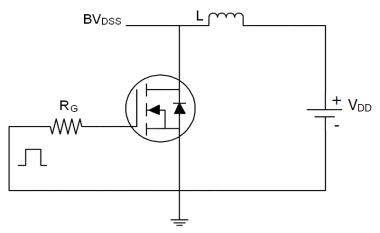
- 1. Repetitive Rating: Pulse width limited by maximum junction temperature.
- **2.** Surface Mounted on FR4 Board, $t \le 10$ sec.
- **3.** Pulse Test: Pulse Width ≤ 300μ s, Duty Cycle ≤ 2%.
- 4. Guaranteed by design, not subject to production

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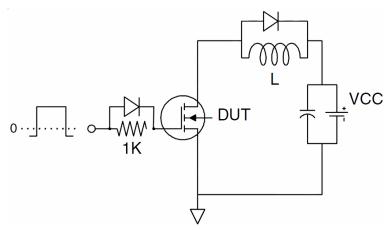


Test Circuit

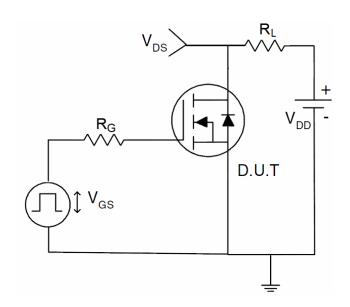
1) E_{AS} Test Circuits



2) Gate Charge Test Circuit:

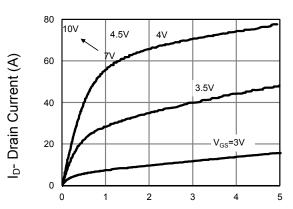


3) Switch Time Test Circuit:



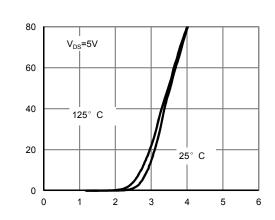


Typical Electrical and Thermal Characteristics (Curves)



Vds Drain-Source Voltage (V)

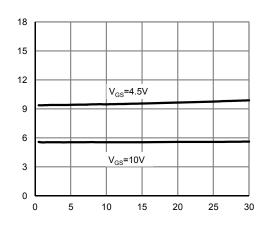
Figure 1 Output Characteristics



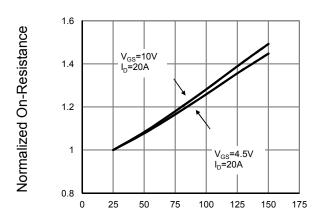
Ip- Drain Current (A)

Rdson On-Resistance Normalized

Vgs Gate-Source Voltage (V)
Figure 2 Transfer Characteristics

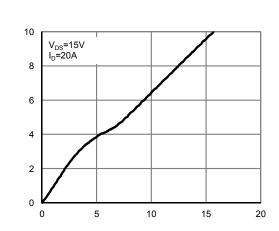


I_D- Drain Current (A) **Figure 3 Rdson- Drain Current**

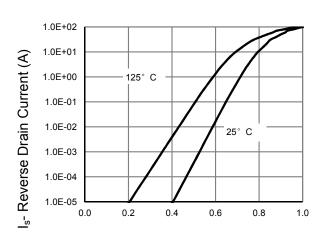


T_J-Junction Temperature(°C)

Figure 4 Rdson-Junction Temperature



Qg Gate Charge (nC)
Figure 5 Gate Charge



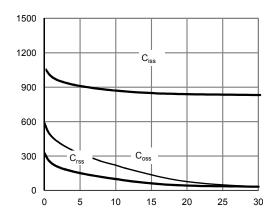
Vsd Source-Drain Voltage (V)

Figure 6 Source- Drain Diode Forward

Vgs Gate-Source Voltage (V)

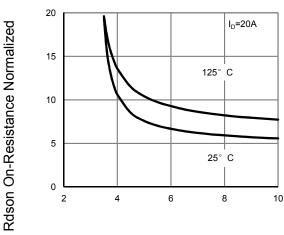






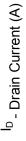
Vds Drain-Source Voltage (V)

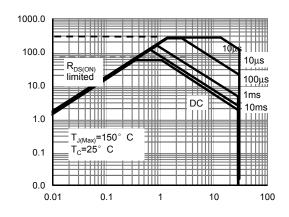
Figure 7 Capacitance vs Vds



Vgs Gate-Source Voltage (V)

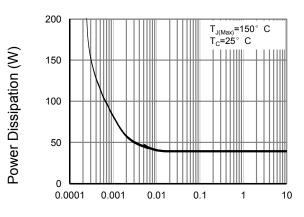
Figure 9: On-Resistance vs. Gate-Source Voltage





Vds Drain-Source Voltage (V)

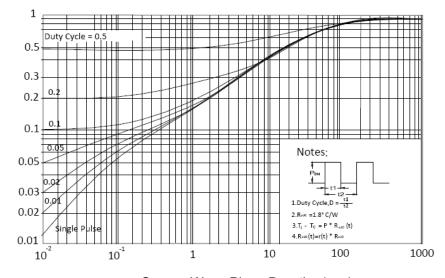
Figure 8 Safe Operation Area



 $T_{J}\text{-Junction Temperature }({}^{\circ}\!\mathbb{C})$

Figure 10 Power De-rating



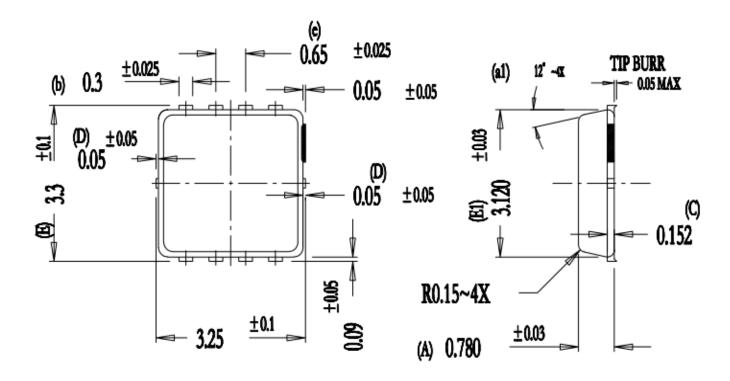


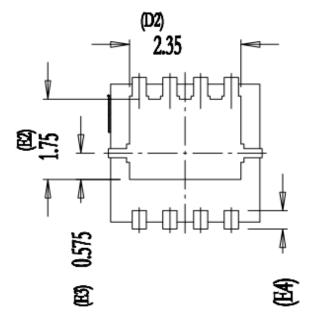
Square Wave Pluse Duration(sec)

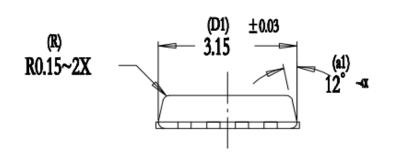
Figure 11 Normalized Maximum Transient Thermal Impedance



DFN3.3*3.3 Package Information







SYMBOL	MILLIMETER			
	MIN	NOM	MAX	
Λ	0.75	0.78	0.81	
A1				
ь	0.297	0.3	0.35	
С	_	0.152		
D	0.00	0.05	0.1	
D1	3.12	3.15	3.18	
D2	_	2.35		
E	3.2	3.3	3.4	
E1	3.09	3.12	3.15	
R2	-	1.75		
E3	_	0.575		
B4				
R	_	0.15		
e	0.65BSC			
al.	_	12'		



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