

FNK N-Channel Enhancement Mode Power MOSFET

Description

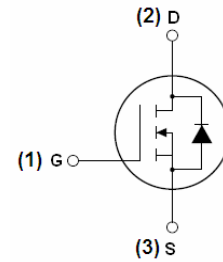
The FNK03N02E uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

- $V_{DS} = 30V, I_D = 140A$
 $R_{DS(ON)} < 3.0\ m\Omega @ V_{GS} = 10V$
 $R_{DS(ON)} < 4.0\ m\Omega @ V_{GS} = 4.5V$
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

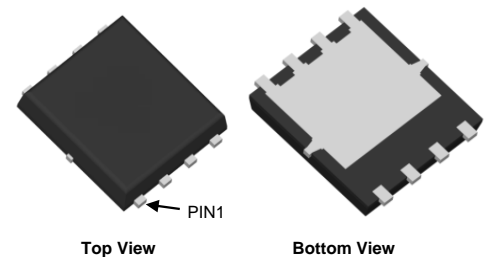
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



Schematic diagram



DFN5X6



Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
FNK03N02E	FNK03N02E	DFN5x6-8L	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	140	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	105	A
Pulsed Drain Current	I_{DM}	560	A
Maximum Power Dissipation	P_D	130	W
Derating factor		0.87	W/ $^\circ C$
Single pulse avalanche energy ^(Note 5)	E_{AS}	240	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	1.15	$^{\circ}\text{C/W}$
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Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

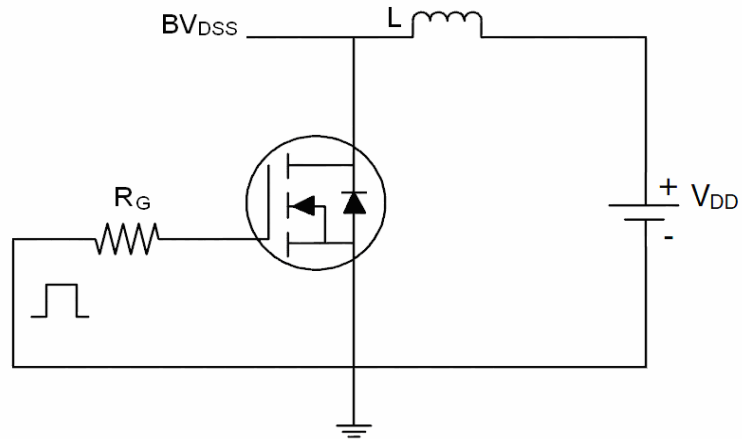
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	30	34	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.0	1.2	2.0	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A	-	2.1	3.4	mΩ
		V _{GS} =4.5V, I _D =10A		2.4	4.0	
Forward Transconductance	g _{FS}	V _{DS} =10V, I _D =20A	32	-	-	S
Dynamic Characteristics ^(Note4)						
Input Capacitance	C _{ISS}	V _{DS} =15V, V _{GS} =0V, F=1.0MHz	-	5400	-	PF
Output Capacitance	C _{OSS}		-	720	-	PF
Reverse Transfer Capacitance	C _{rss}		-	560	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =15V, I _D =2A, R _L =15Ω V _{GS} =10V, R _G =2.5Ω	-	26	-	nS
Turn-on Rise Time	t _r		-	24	-	nS
Turn-Off Delay Time	t _{d(off)}		-	91	-	nS
Turn-Off Fall Time	t _f		-	39	-	nS
Total Gate Charge	Q _g	V _{DS} =15V, I _D =30A, V _{GS} =10V	-	38		nC
Gate-Source Charge	Q _{gs}		-	9		nC
Gate-Drain Charge	Q _{gd}		-	13		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V, I _S =150A	-		1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	150	A
Reverse Recovery Time	t _{rr}	TJ = 25°C, IF = 20A	-	42	-	nS
Reverse Recovery Charge	Q _{rr}	di/dt = 100A/μs ^(Note3)	-	39	-	nC

Notes:

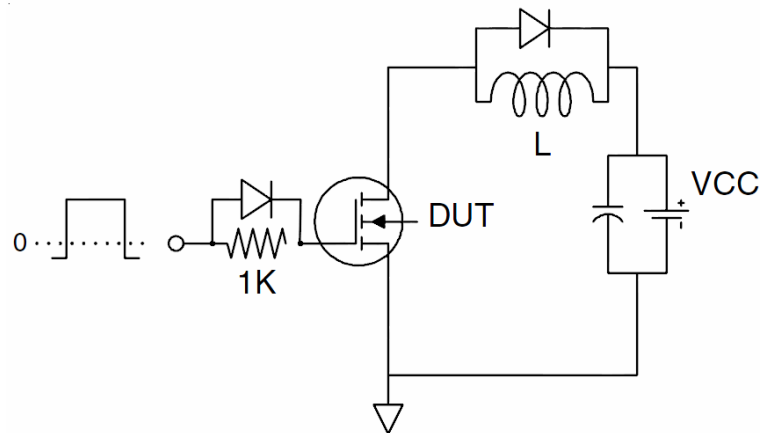
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. E_{AS} condition : $T_J=25^{\circ}\text{C}, V_{DD}=20V, V_G=10V, L=0.5mH, R_g=25\Omega, I_{AS}=58.5A$

Test circuit

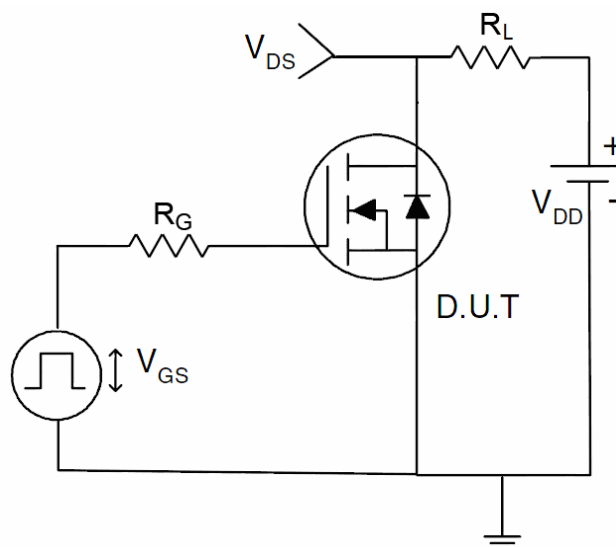
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

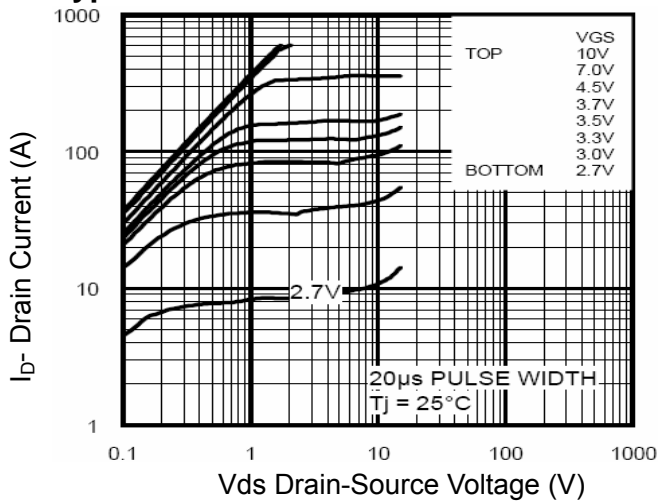


Figure 1 Output Characteristics

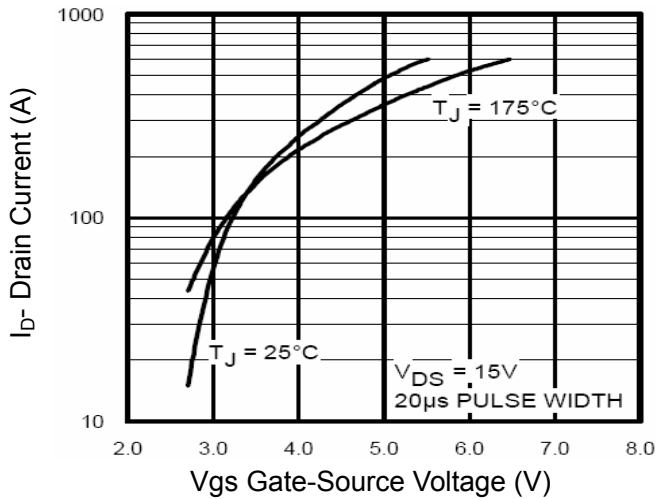


Figure 2 Transfer Characteristics

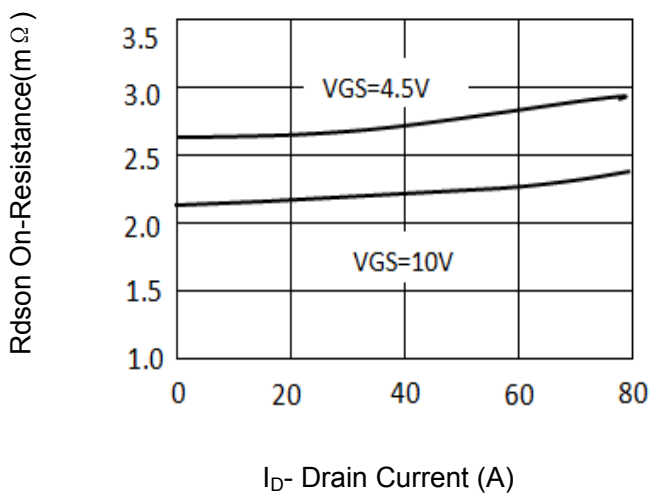


Figure 3 Rdson- Drain Current

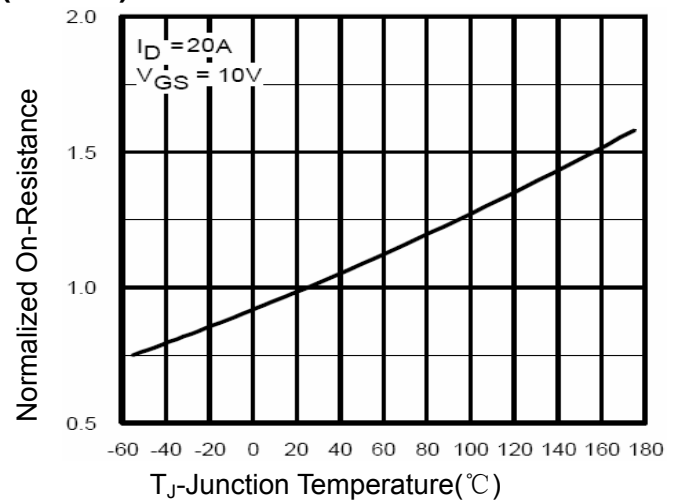


Figure 4 Rdson-Junction Temperature

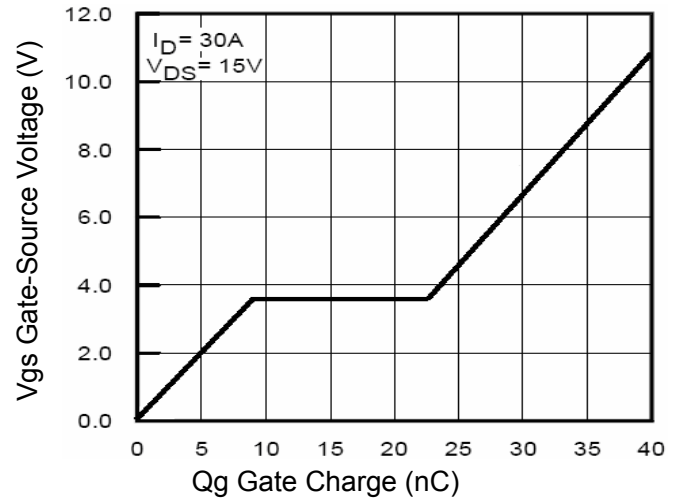


Figure 5 Gate Charge

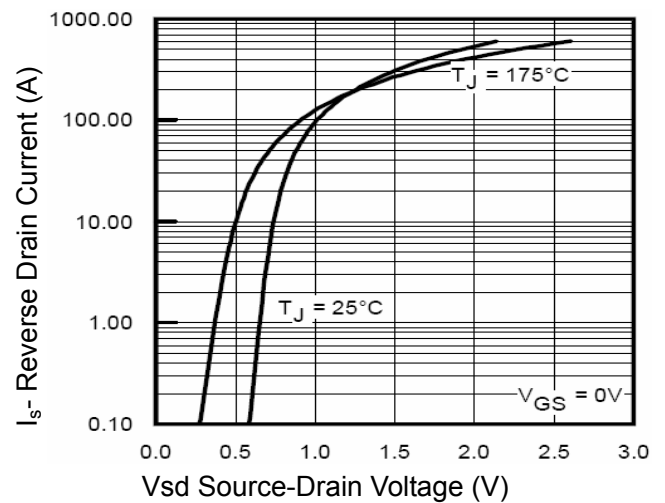


Figure 6 Source- Drain Diode Forward

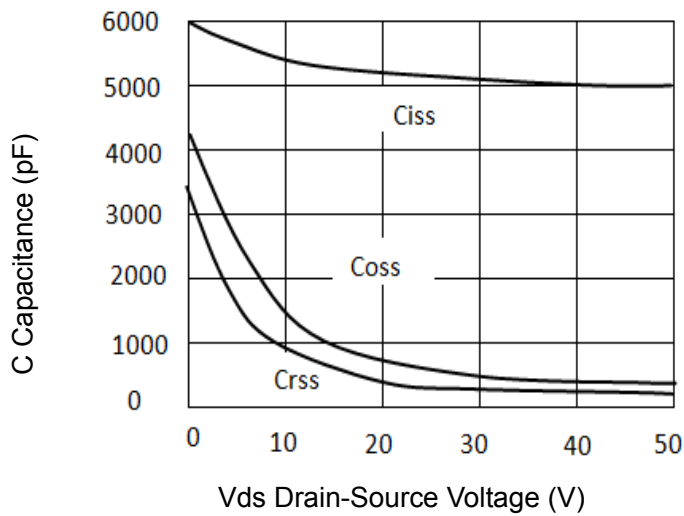


Figure 7 Capacitance vs Vds

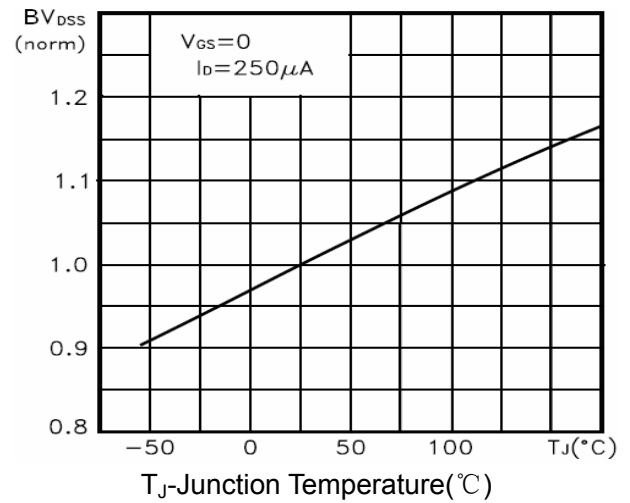


Figure 9 BV_{DSS} vs Junction Temperature

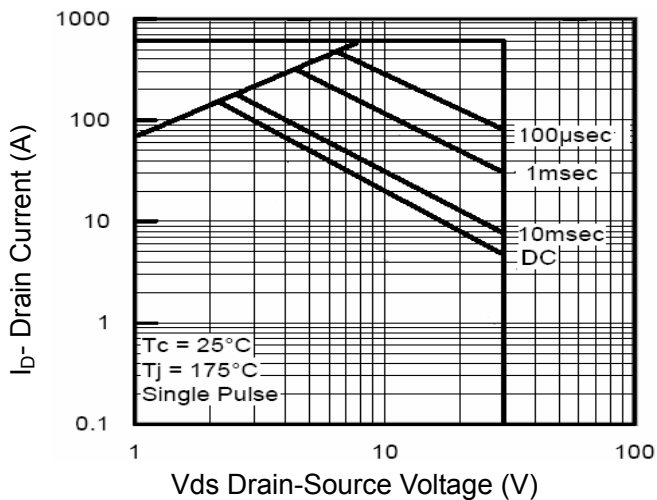


Figure 8 Safe Operation Area

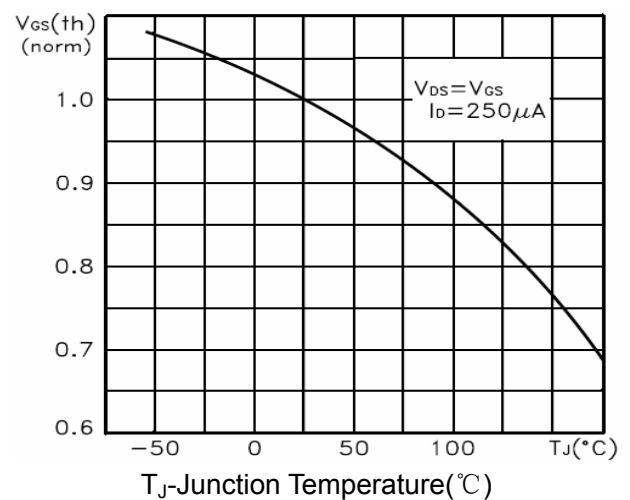


Figure 10 V_{GS(th)} vs Junction Temperature

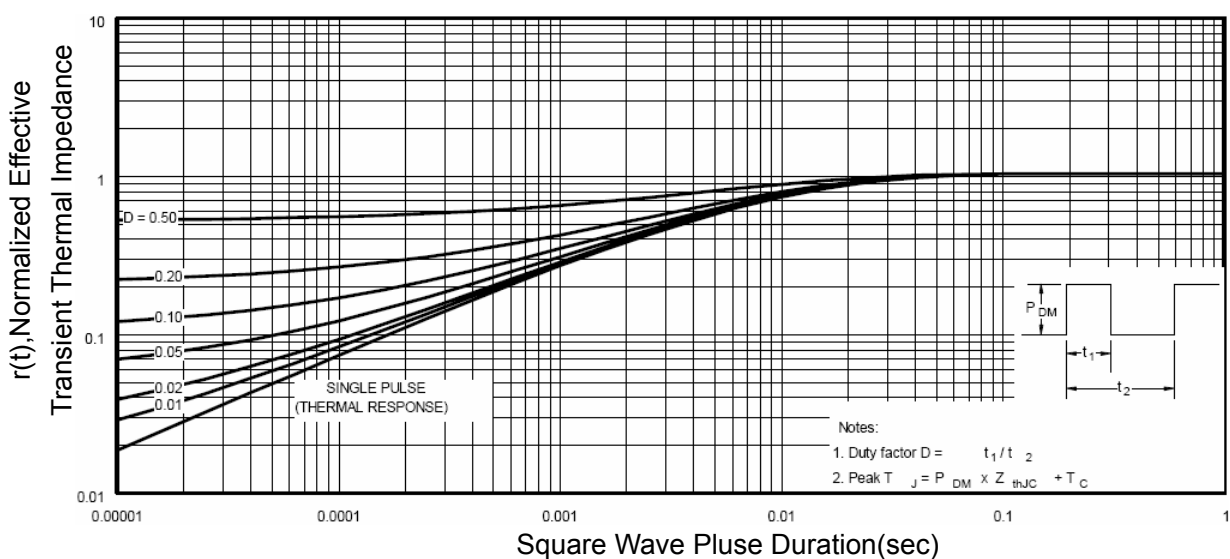
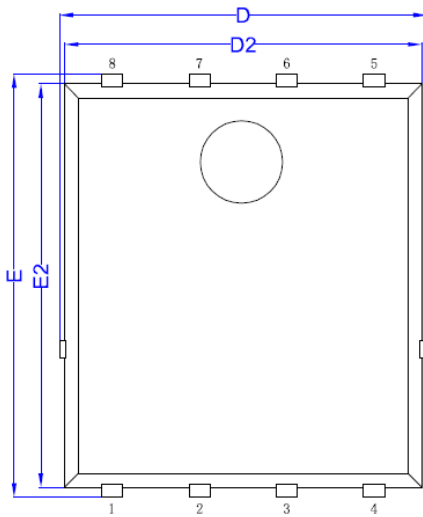


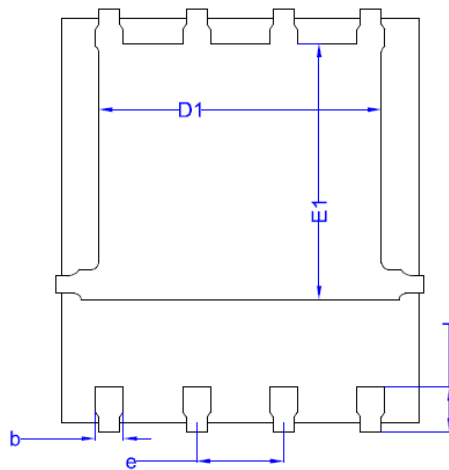
Figure 11 Normalized Maximum Transient Thermal Impedance

DFN5X6-8L Package Information

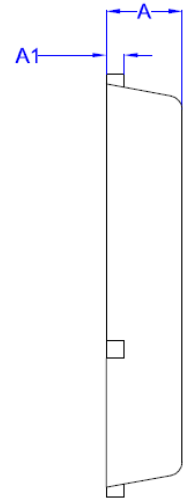
Top View



Bottom View



Side View



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.00	1.10	1.20
A1	0.254 BSC		
D	5.15	5.35	5.55
E	5.95	6.15	6.35
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
e	1.27BSC		
b	0.31	0.41	0.51
L	0.56	0.66	0.76

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