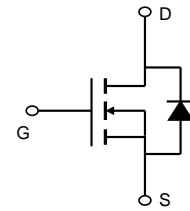


General Description

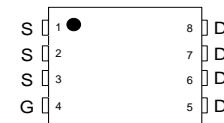
- Trench Power MOSFET technology
- Low $R_{DS(ON)}$
- Low Gate Charge
- RoHS and Halogen-Free Compliant

Product Summary

V_{DS}	20V
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 2.5m Ω
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	< 2.8m Ω
$R_{DS(ON)}$ (at $V_{GS}=2.5V$)	<4.0m Ω



Schematic diagram



Marking and pin Assignment

Applications

- Load switch, battery switch in portable devices

Orderable Part Number		Package Type	Form	Minimum Order Quantity	
FNK02N018E		DFN5*6	Tape & Reel	5000	
Absolute Maximum Ratings T _A =25°C unless otherwise noted					
Parameter		Symbol	Maximum		Units
Drain-Source Voltage		V _{DS}	20		V
Gate-Source Voltage		V _{GS}	±12		V
Continuous Drain Current ^G		I _D	180		A
Pulsed Drain Current ^C		I _{DM}	720		
Continuous Drain Current		I _{DSM}	60		A
Avalanche energy L=0.05mH ^C		E _{AS}	123		mJ
Power Dissipation ^B		P _D	56		W
Junction and Storage Temperature Range		T _J , T _{STG}	-55 to 150		°C
Thermal Characteristics					
Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	t ≤ 10s	R _{θJA}	25	30	°C/W
Maximum Junction-to-Ambient ^{A D}	Steady-State		50	60	°C/W
Maximum Junction-to-Case	Steady-State	R _{θJC}	1.8	2.2	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	20			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =20V, V _{GS} =0V			1	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±12V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	0.5	0.75	1.1	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =30A		1.5	2.5	mΩ
		V _{GS} =4.5V, I _D =20A		1.8	2.8	mΩ
		V _{GS} =2.5V, I _D =15A		2.8	4.0	mΩ
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.6	1	V
I _S	Maximum Body-Diode Continuous Current				50	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		5000		pF
C _{oss}	Output Capacitance			1450		pF
C _{rss}	Reverse Transfer Capacitance			200		pF
R _g	Gate resistance	f=1MHz	0.3	0.7	1.5	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =20A		78	110	nC
Q _g (4.5V)	Total Gate Charge			36	50	nC
Q _{gs}	Gate Source Charge			10		nC
Q _{gd}	Gate Drain Charge			10		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =0.75Ω, R _{GEN} =3Ω		9		ns
t _r	Turn-On Rise Time			8		ns
t _{D(off)}	Turn-Off DelayTime			85		ns
t _f	Turn-Off Fall Time			18		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, di/dt=500A/μs		21		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, di/dt=500A/μs		57		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{DSM} is based on R_{θJA} ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T_{J(MAX)}=150° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

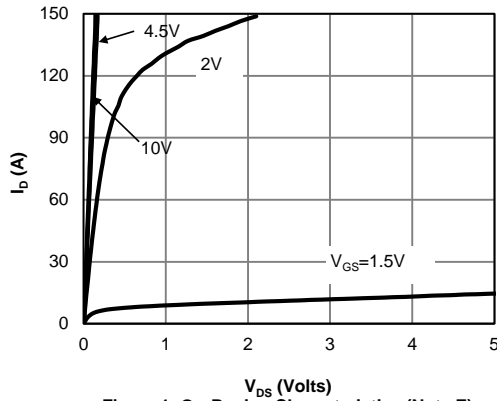


Figure 1: On-Region Characteristics (Note E)

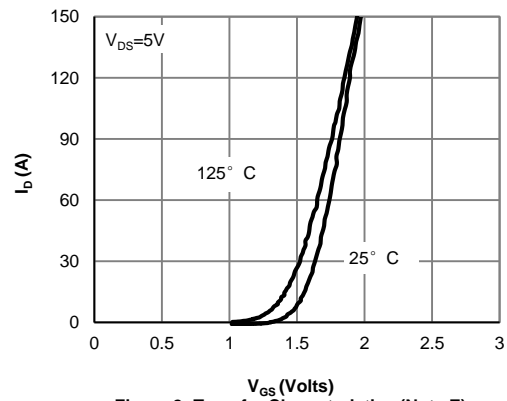


Figure 2: Transfer Characteristics (Note E)

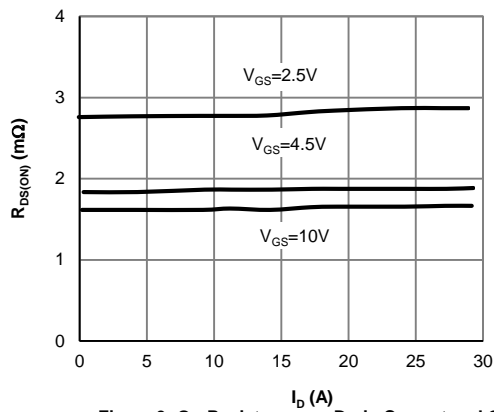


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

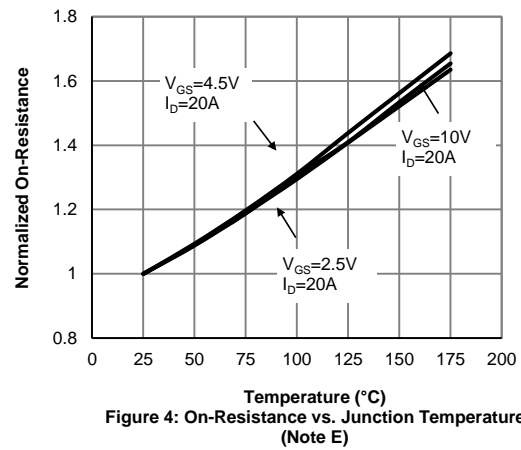


Figure 4: On-Resistance vs. Junction Temperature (Note E)

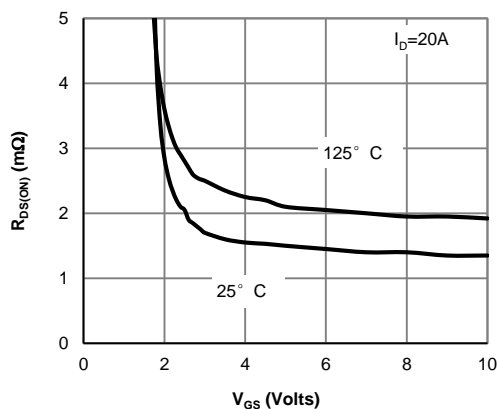


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

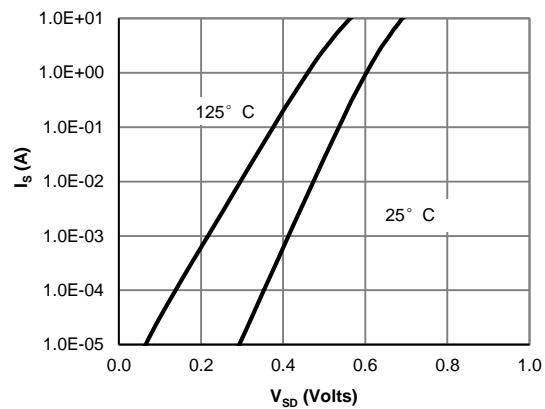


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

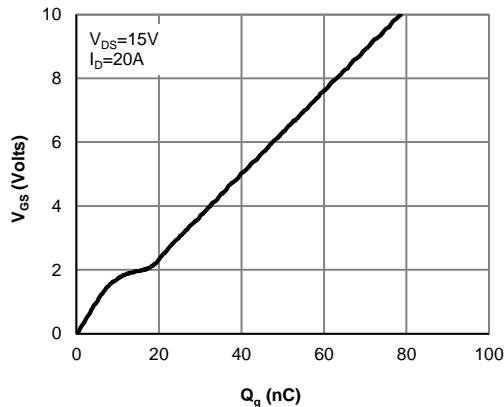


Figure 7: Gate-Charge Characteristics

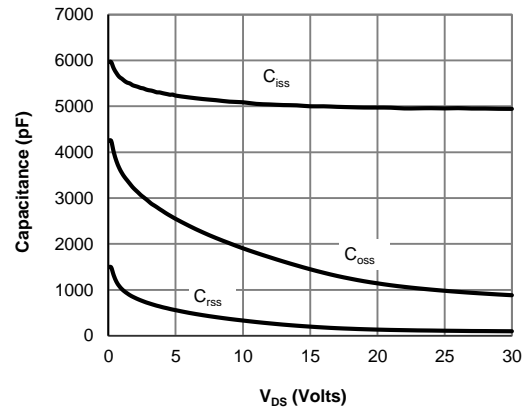


Figure 8: Capacitance Characteristics

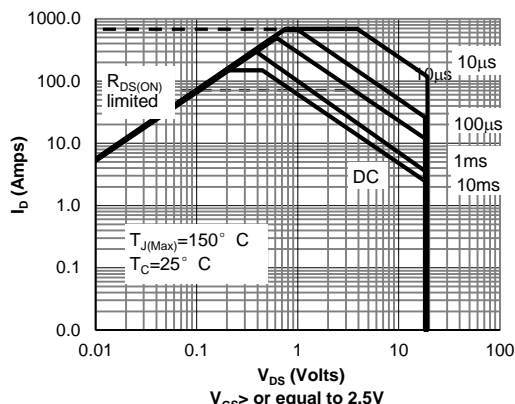


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

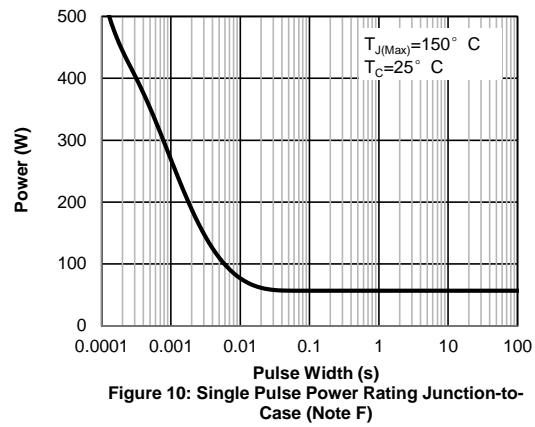


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

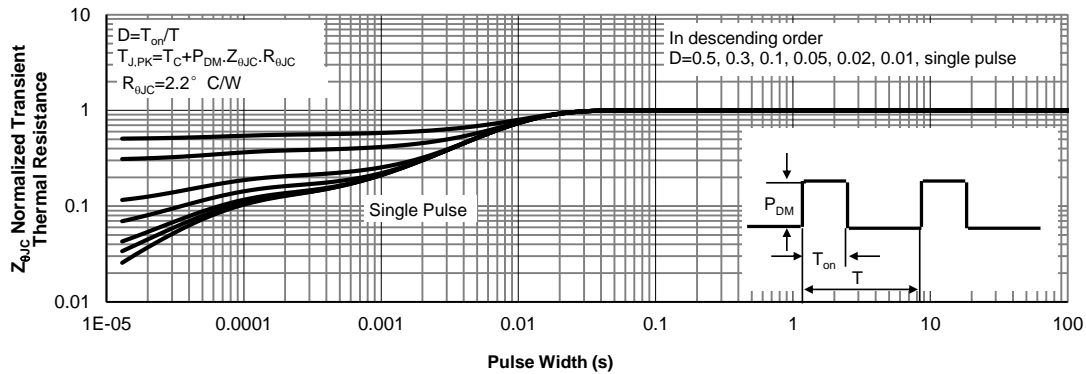


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

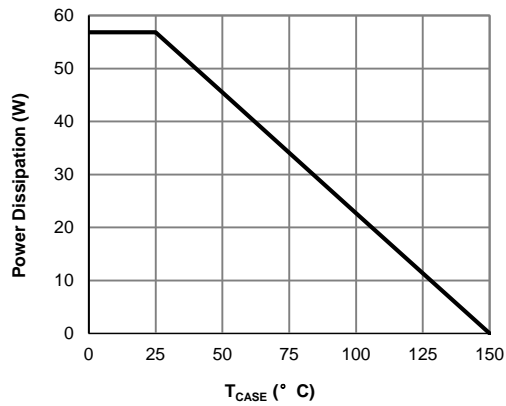


Figure 12: Power De-rating (Note F)

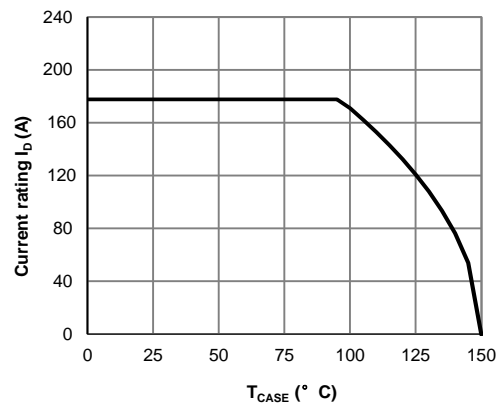


Figure 13: Current De-rating (Note F)

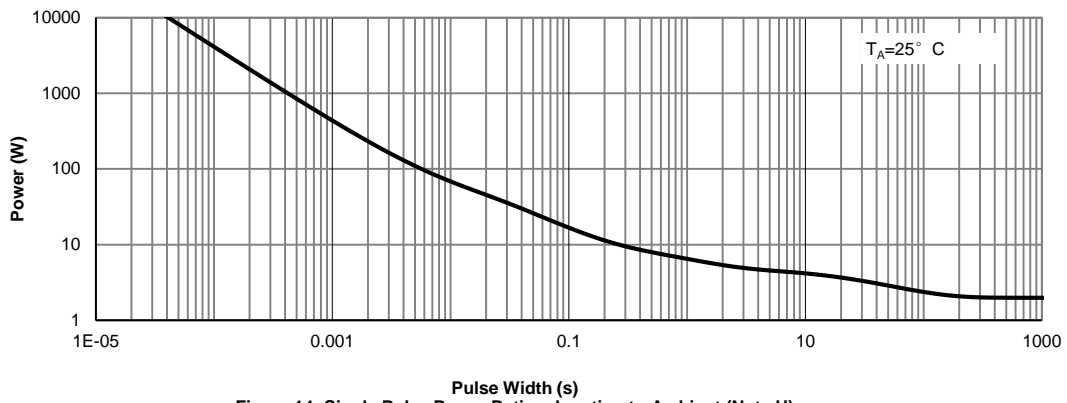


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

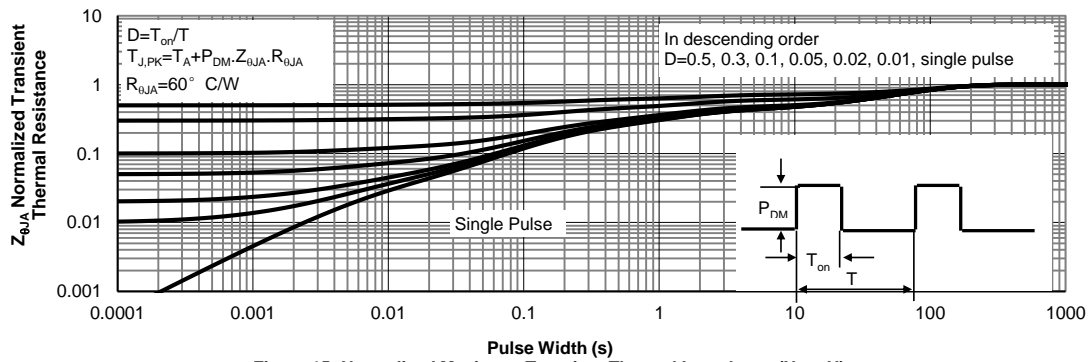
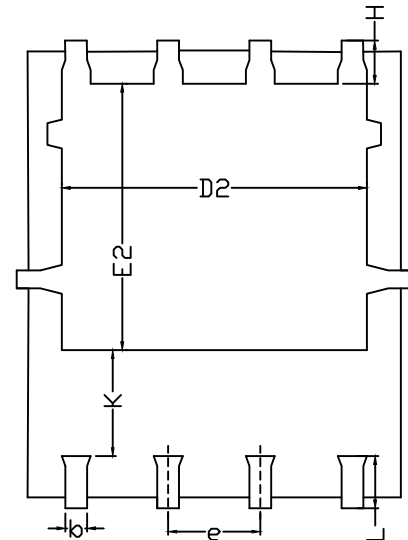
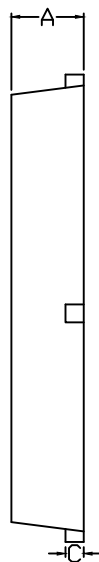
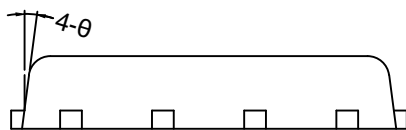
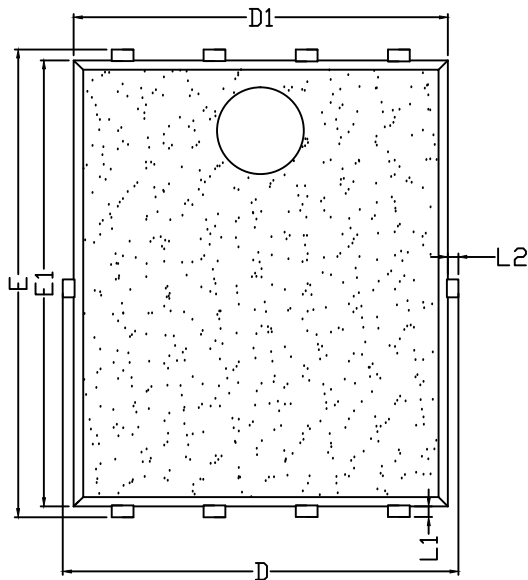


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

DFN5X6 Package Information



SYMBOL	mm		
	MIN	NOM	MAX
*A	0.90	0.95	1.00
*b	0.25	0.30	0.35
*c	0.20	0.25	0.30
D	5.15BSC		
*D1	4.90	5.00	5.10
D2	3.90	4.05	4.20
*e	1.17	1.27	1.37
E	6.15BSC		
*E1	5.75	5.85	5.95
E2	3.35	3.50	3.65
H	0.51	0.61	0.71
K	1.10	–	–
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
L2	–	–	0.12
P	0.95	1.10	1.25
θ	9°	11°	13°

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