

General Description

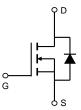
- Shielded Gate Transistor Power MOSFET
- Combined of low $R_{\text{DS}(\text{ON})}$ and wide safe operatiing area (SOA)

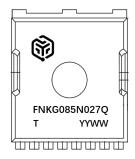


Applications

 Load switch • BMS Motor

V _{DS}	85V
I _D (at V _{GS} =10V)	198A
R _{DS(ON)} (at V _{GS} =10V)	< 2.7mΩ





TOLL Bottom View Top View D s PIN1(G) PIN1(G)

Orderable Part Number	Package Type	Form	Minimum Order Quantity
FNKG085N027Q	TOLL	Tape & Reel	
Absolute Maximum Ratings T _A =25°C	unless otherwise noted		
Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V _{DS}	85	V
Gate-Source Voltage	V _{GS}	±20	V
Continuous Drain Current	I _D	198	A
Pulsed Drain Current ^c (≤100µS)	I _{DM}	790	
Avalanche energy L=0.3mH ^C	E _{AS}	400	mJ
Power Dissipation ^B	P _D	190	W
Power Dissipation ^A	P _{DSM}	10	W
Junction and Storage Temperature Ran	ge T _J , T _{STG}	-55 to 175	°C

Thermal Characteristics						
Parameter		Symbol	Тур	Max	Units	
Maximum Junction-to-Ambient ^A	t ≤ 10s	R	10	15	°C/W	
Maximum Junction-to-Ambient AD	Steady-State	$R_{ extsf{ heta}JA}$	35	45	°C/W	
Maximum Junction-to-Case	Steady-State	$R_{ ext{ heta}JC}$	0.65	0.83	°C/W	





Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Тур	Max	Units
	PARAMETERS		-		-	<u>e</u>
BV_{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	85			V
I _{DSS}	Zero Gate Voltage Drain Current	V_{DS} =100V, V_{GS} =0V			1	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	$V_{DS}=V_{GS,}I_{D}=250\mu A$	2.0	2.8	4.0	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A		1.8	2.7	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		50		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V			1	V
DYNAMI	C PARAMETERS			I		<u> </u>
C _{iss}	Input Capacitance			6550		pF
C _{oss}	Output Capacitance	V _{GS} =0V, V _{DS} =40V, f=1MHz		1450		pF
C _{rss}	Reverse Transfer Capacitance			60		pF
R _g	Gate resistance	f=1MHz		2.5	5	Ω
SWITCH	ING PARAMETERS		-	-	-	<u> </u>
Q _g (10V)	Total Gate Charge			85	105	nC
Q _{gs}	Gate Source Charge	V _{GS} =10V, V _{DS} =50V, I _D =20A		35		nC
Q _{gd}	Gate Drain Charge	7		25		nC
Q _{oss}	Output Charge	V _{GS} =0V, V _{DS} =50V		240		nC
t _{D(on)}	Turn-On DelayTime			25		ns
t _r	Turn-On Rise Time	V _{GS} =10V, V _{DS} =50V, R _L =3.75Ω,		22		ns
t _{D(off)}	Turn-Off DelayTime	$R_{GEN}=3\Omega$		51		ns
t _f	Turn-Off Fall Time	7		25		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, di/dt=500A/μs		82		ns
Q _{rr}	Body Diode Reverse Recovery Charge	_P I _F =20A, di/dt=500A/μs		820		nC

A. The value of R_{0JA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^{\circ}$ C. The Power dissipation P_{DSM} is based on R _{0JA} t≤ 10s and the maximum allowed junction temperature of 175° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175° C may be used if the PCB allows it.

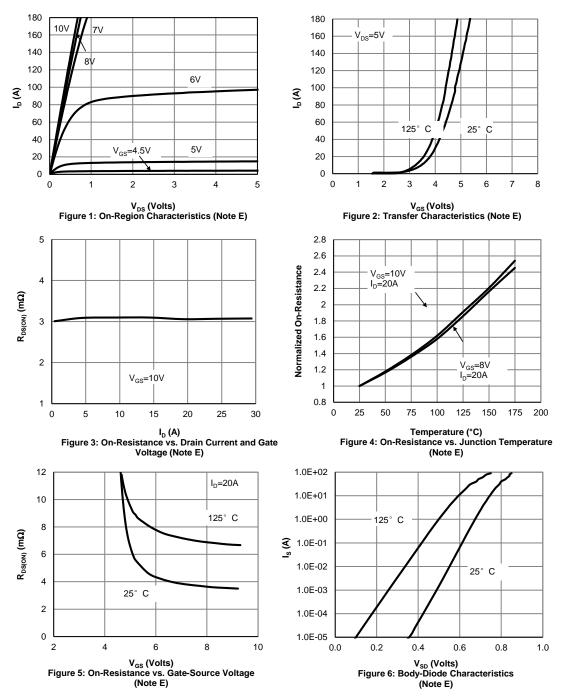
B. The power dissipation P_{D} is based on $T_{J(MAX)}=75^{\circ}$ C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature $T_{J(MAX)}$ =175° C. D. The R_{0JA} is the sum of the thermal impedance from junction to case R_{0JC} and case to ambient. E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max. F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$ =175° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited. H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}$ C.

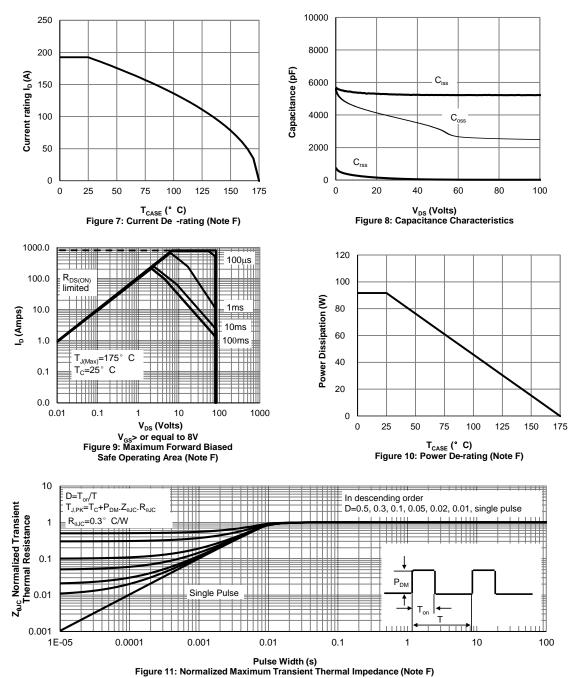


TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS





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FNKG085N027Q

Figure A: Gate Charge Test Circuit & Waveforms

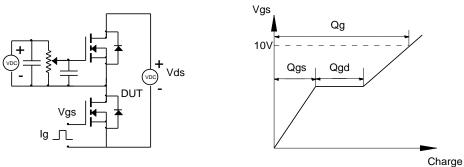


Figure B: Resistive Switching Test Circuit & Waveforms

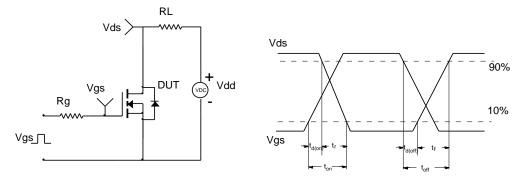


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

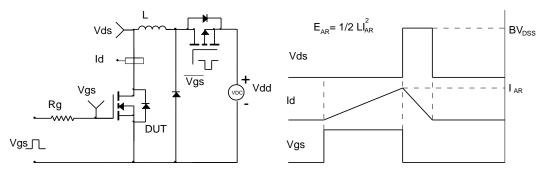
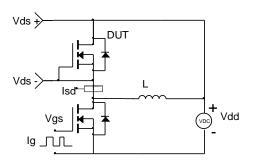
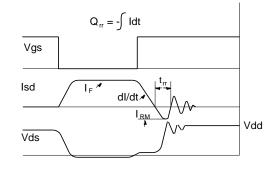
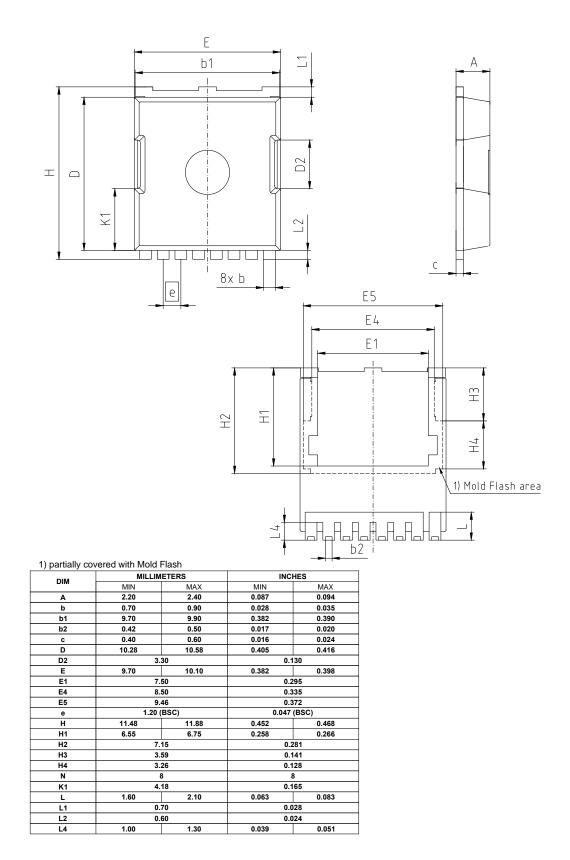


Figure D: Diode Recovery Test Circuit & Waveforms











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